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proceedings

Second Conference
on the
NAVY MICROELECTRONICS PROGRAM

Washington, D.C.
September 24, 25, 26, 1962

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Second Conference
on the
NAVY MICROELECTRONICS PROGRAM

Washington, D.C.
September 24, 25, 26, 1962

Sponsored by

OFFICE OF NAVAL RESEARCH
and
NAVAL RESEARCH LABORATORY

Office of Naval Research
Department of the Navy
Washington, D.C.

PREFACE

This document contains the proceedings of the Second Conference on the Navy Microelectronics Program held on September 24, 25, 26, 1962. The first day's meeting was held at the Naval Research Laboratory and the second and third day at the Auditorium of the Department of the Interior, Washington, D.C.

About one hundred thirty-five representatives of the Navy Department and other federal agencies attended the session at NRL, and some three hundred seventy-five representatives of industry joined them in the sessions at the Department of Interior.

The Conference was divided into three parts, covering reports and discussions of the Navy in-house program in microelectronics on the first day, reports on selected Navy contracts related to microelectronics on the second day, and a general summary of the microelectronics programs and plans of the Bureaus and Office of Naval Research on the last day.

Capt. A. E. Krapf, Director of the Naval Research Laboratory, made the facilities and hospitality of the Laboratory available for the first day of this Conference and helped start the proceedings with an inspiring message. It was rewarding to commence this three-day meeting at NRL, the Navy's primary research laboratory, with the opening sessions devoted to Navy laboratory business.

Mr. Albert Brodzinsky, Superintendent of the Electronics Division, NRL, in serving as general chairman of the Conference, conducted a smooth operating and efficient meeting in which he was assisted by the following session chairmen:

John E. Davey, Naval Research Laboratory
Capt. S. F. Balaban, USN, Office of Naval Research
L. Schlesinger, Bureau of Naval Weapons
N. J. Smith, Office of the Chief of Naval Operations

Rear Admiral B. F. Roeder, Director of Naval Communications, presented the keynote address at the opening of the principal session of the Conference, which was held on the second day and was attended by both government and industry personnel, totalling over 500.

The many government and industry participants, whose names appear under the many titles appearing in this document, are those who in the final analysis made this Conference at all workable. They are the primary "doers" who have been directing or carrying out the research and who have then reported on it at the Conference.

The assistance and suggestions of all those who contributed to the success of the Conference are gratefully acknowledged. Special thanks are due the "men behind the scenes" at NRL and ONR whose expert handling of the physical arrangements made this an unusually smooth running Conference.

RE Wiley

February 1963

R. E. Wiley
Assistant Research Coordinator
Office of Naval Research

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NAVY LABORATORY REPORTS

Chairman: John E. Davey
Naval Research Laboratory

Naval Research Laboratory
September 24, 1962

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MICROELECTRONICS CONFERENCE

WELCOME

CAPT A. E. Krapf, Director
U. S. Naval Research Laboratory
Washington, D. C.

Good morning ladies and gentlemen. It is indeed a pleasure to welcome you to the Naval Research Laboratory. I am not going to try to go into the importance of the subject of microelectronics and its position in the Navy today. I think that's probably what you're here for. A great deal has been accomplished, but there is more to be done in this business of Microelectronics.

The Laboratory is proud to offer its facilities to you and to have you here with us. We certainly hope that your meeting is a success.

Some of you I am sure are reasonably well acquainted with the Naval Research Laboratory, its overall program, its staff, and the work that it is doing. I might just take a minute to bring the others up to date. The Laboratory was established in 1923 as a result of a recommendation by our good friend, Thomas Edison, who decided at that time that the Navy should have an activity that could work on and attempt to solve some of the problems facing the Navy; short-range problems and long-range problems. And indeed, the mission as laid down by Thomas Edison is still the mission of the Laboratory today. Our 3,200 personnel, including 1,100 professionals, are engaged in doing just that.

Our total 56 million dollar budget is composed of two basic portions. Approximately half of it is used for the short-range day-by-day problems assigned to the Laboratory by the various technical bureaus and offices of the Navy, and also by activities outside of the Navy. The other 50 percent of our basic budget is used to support the fundamental long-range research work here at the Laboratory. It is provided to us by our management Bureau, the Office of Naval Research. The program it supports is generated by scientists of the Laboratory and approved by the Chief of Naval Research.

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As you know, the Naval Research Laboratory has always had a very strong electronics program. This stems right back to the start of the Laboratory when, in order to organize and get it started in 1923, several other groups were moved in, particularly a group that was working in aircraft radio or aircraft wireless. They were moved in as one nucleus of the Laboratory staff under Dr. A. Hoyt Taylor. Then a group under Dr. Hayes was moved in from the Engineering Experiment Station where they had been doing underwater sound work.

Prior to World War II and during that war this Laboratory made many contributions to the electronic art, including the development of radar as we know it now. So you can see that a subject like microelectronics is very dear to the hearts of a good many of the Laboratory members. I think it is proper and I hope will be beneficial to this Conference that you are holding it here at the Naval Research Laboratory.

Good luck to you and I certainly hope that your Conference will be a success.

INTRODUCTORY REMARKS

CAPT J. M. Ballinger, USN
Deputy and Assistant Chief of Naval Research

On behalf of the Office of Naval Research I want to welcome you to the second Conference on the Navy Microelectronics Program. This year the conference has been extended one day as an indication of the growing importance of this program. During these three days you will get a comprehensive and thorough look at not only what the Navy laboratories but also what the leading industrial firms are accomplishing on this exciting new frontier of research.

There is no area of technology in which developments have come so rapidly in the postwar era as in electronics. The military systems in operation today and under development for the future are so sophisticated that in comparison our World War II equipment seems like something out of the stone age. The reason for this rapid postwar progress can be expressed in one word–research.

The Navy has played a leading role in electronics research and is greatly concerned that such research continue to be pressed to try to fill the apparently bottomless maw of our electronic needs. As you well know, virtually every major weapon and piece of equipment in the Fleet today needs a reliable electronic nervous system for its operation. Furthermore, we are demanding new advanced systems capable of performing tasks that might have been considered fantastic a few years ago.

We must have electronic reconnaissance systems complete with high speed computers capable of rapid and accurate determination at long range of the character, location and identity of enemy targets. We need surveillance systems that can shift rapidly from active to passive or semiactive modes of operation as well as active systems capable of quick frequency shifts. We require jamming systems that cannot be by-passed and deception systems immune to enemy analysis and solution.

As if these challenges were not formidable enough, we have additional requirements. We must have these systems in black boxes small enough to pack into an aircraft or missile airframe without significantly increasing the weight. They must also be compact enough to fit into shipboard compartments without forcing us to build bigger ships to contain the equipment together with its operating personnel.

This is where microelectronics comes in and, since there are special and in some cases unique Navy needs, this is why we are dependent on the Navy laboratories to help us solve these problems. It is your background, experience, and intimate knowledge of the sea and ship environments that we need to guide us in the development of microelectronic components that will work not only in a laboratory but under all the varied operating conditions encountered by our Fleet.

Smallness and lightness are not the only objectives of microelectronics. We have to be equally concerned with reliability and cost. We still have to determine whether the best approach to reliability is redundancy circuits or whether we must have completely new concepts.

In this connection, we must also consider the fact of complexity. It is well known that it is becoming increasingly difficult to obtain highly skilled personnel to operate the advanced electronics equipment now being installed in the Fleet. Long life reliability is one way of easing the problem by reducing the amount and frequency of maintenance, but what we really need is equipment that can be operated by those who are less than graduate engineers.

We would also like to be able to use fewer men and perhaps reverse the trend of recent years. In 1940 a destroyer required 13 men to operate and maintain communications, fire control and similar equipment. A modern frigate uses 97 men, and when the Naval Tactical Data System installation is included, a total of 119 men is needed for the operation and maintenance of all electronics equipment on such a ship.

A similar comparison illustrates the increasing cost of electronics systems. In 1940 the installed electronic gear on a destroyer cost about $430,000 or about 0.35 percent of the initial cost of the ship. In 1960 the cost for a destroyer of similar tonnage had increased to $6 million or about 15.4 percent of the total cost of the destroyer.

The Office of Naval Research has had a long interest in microelectronics. In fact, it was the Army-Navy Instrumentation Program, initiated several years ago by ONR, which established the first major need for the microminiaturization of electronic components. An integrated and simplified cockpit instrument display, which gives the pilot on television-type displays all the information he needs for navigating and manuevering his aircraft, awaits further advances in miniaturization.

It is our hope that this meeting will bring forth and stimulate new ideas in microelectronics which will bring us nearer to our objective. Already for the first time we now see the possibility of operational applications of microelectronics. The road ahead is still plenty bumpy but at least we can see where it is going.

I want to congratulate you on what you have accomplished so far. If it is indicative of what will be done in the future, we might well be optimistic that the Navy will continue to lead the way in this rapidly burgeoning field.

MICROELECTRONIC APPLICATIONS PROGRAM

Howard B. Martin
U.S. Naval Air Development Center
Johnsville, Pa.

The microelectronics program at the Naval Air Development Center is sponsored by the Avionics Branch, BuWeps. Since the Center has responsibilities to other BuWeps groups, however, the benefits will not be restricted solely to Avionics Branch programs. The prime objective of our program is to expedite the application of microelectronics to systems. These systems include both those developed at the Center and those developed by BuWeps contractors. This prime objective may be divided and subdivided into fragments, but, for the sake of convenience, we may say that it has three important elements:

1. Development of an in-house capability in microelectronic techniques and in the application of microelectronics to systems.
2. Review of proposed system applications of microelectronics.
3. Dissemination of information on microelectronics to BuWeps Avionics contractors and potential contractors.

In the development of our in-house capability in microelectronic techniques we have chosen the thin film approach since it is most suitable for the expeditious fabrication of prototype microcircuitry for in-house systems development programs. The in-house thin film effort will be described by Mrs. Drautman in the following paper.

Throughout the history of electronics the introduction of a radically new component or technique generally has had a traumatic effect on systems designers. The introduction of transistors and printed wiring are excellent examples. In all cases, however, after familiarization periods of various lengths, the systems designers bow to the inevitable and learn to adapt the new component or technique, and it is ultimately used in their designs. The introduction of microelectronics, far from being an exception to the rule, is proving to be a classic example of the effect since it represents not only a new component or a new technique, but an entirely new concept in systems design. As an activity concerned primarily with systems design the Naval Air Development Center must suffer through these birth pains along with industry and part of our job in the Development Support Division, Aeronautical Electronic and Electrical Laboratory, is to help ease the birth pains thereby hastening the introduction of microelectronics into our systems. Since we are unable to run a formal educational program in microelectronics techniques and applications, our principal effort is to utilize symposia or presentations made by manufacturers as a means of familiarizing key systems personnel with the various approaches to microelectronics might be effectively applied. Perhaps the most difficult part of this job is to convince people that, the principal benefit to be derived from the application of microelectronics is not the reduction of size and weight, but the improvement of reliability, and that it should be viewed primarily as a tool for reliability improvement. To date, many of the key systems personnel have acquired a sufficient understanding of microelectronics to enable them to start theinking of specific applications. This process will, of course, be accelerated when our thin film effort will be able to supply the systems groups with prototype microcircuitry.

Various systems groups at the Center, as a part of their responsibility to BuWeps, are required to review bidder's proposals and contractor's engineering change proposals. Since most of these proposals now are concerned with microelectronics to some degree, we assist the systems groups in the evaluation of these proposals. In this review, we are concerned with the feasibility of the proposed application, assessment of potential logistic support problems, and adherence to BuWeps microelectronic application policies. Feasibility, in this case, concerns itself with the suitability of a given technique for a specific circuit function. In some cases the organization making the proposal, acting either in good faith or taking a calculated risk, assumes that at some future date a certain circuit function will be realizable using a certain technique. This is perhaps the haziest area in which we operate since we are matching one educated guess, ours, with another, the proposers. We would much rather not play this game, but, since factors such as this might determine the success or failure of the whole system, we feel that it is necessary to point out areas where in our judgement differs from that of the proposer.

Particularly in the area of solid state integrated circuits, microelectronics is at the present largely a single-source proposition. This situation is likely to remain with us until we have an effective standardization program that will focus competitive industry forces on a relatively small number of items having a large market potential. At the present time the most that we can do is to inform the systems group that there is a problem of single source replacement, and attempt to assess the magnitude of the problem in the specific case. It is rather obvious that some of these initial applications should be the focus of early standardization efforts.

The third factor, adherence to BuWeps microelectronic application policies, is concerned with desirable characteristics that have not, as yet, been formally documented, and includes such factors as the inclusion of automatic trouble shooting of fault location provisions, reliability assurance provisions for the microelectronic elements, ease of repair, etc. The sum total of this review may or may not have an effect on the contract award since they are only a few of the factors that must be considered, but, in any event, they give the cognizant systems engineer a picture of the microelectronic state of the art in his system, and a clear understanding of the problems that he may have to face when the development work begins. The requirement for this proposal review should diminish as Center personnel become better acquainted with microelectronics, but in the mean time, while it does not represent a large undertaking in the sense of the man-years of effort involved, it exerts a very direct influence on the design and construction of future avionics systems and is therefore of considerable importance.

As far as effort is concerned, our major endeavor at the present time is serving as an information source on microelectronics to BuWeps contractors and potential contractors. In relation to the proposal review discussed above, this might be considered "service after the sale". We maintain a state of the art surveillance of industry and government microelectronic activities and, based on extensive laboratory evaluation of commercially available microelectronic hardware, generate application engineering data usable by contractors and potential contractors. The information is disseminated through a newsletter, entitled μ-Notes, which is issued approximately monthly and distributed to the industry. With a circulation policy of not more than one copy per address, the current distribution is approximately 250 copies; most of which are directed to systems manufacturers.

In the evaluations of the commercially available items we try to determine the basic worth of the particular item by measuring its performance under all rated operating conditions. This is necessary to verify the information presented by the manufacturer in his data sheet, and, since most data sheets are inadequate in some degree, to extract and publish the most significant data. The bulk of our experience has thus far been in digital circuits and there are great differences in the data sheets published by different manufacturers. None of them are fully adequate, but some give no data at all against which device performance may be measured. Furthermore, there is a lack of standardization of terminology that makes the users job even more difficult. If we succeed in accomplishing nothing more, we feel that if we can introduce standard terminology for digital functions and convince the device manufacturers to improve their data sheets, we will be successful. Another facet of the evaluation program is the determination of possible application difficulties; informing the potential users of these difficulties and recommending means whereby the difficulties may be eliminated or their effects minimized. An example of these potential difficulties is the noise sensitivity exhibited by some logic configurations. Failure to recognize these problems, and consider them in design, could lead to major problems on a system scale. In these potential problem areas we will work very closely with the manufacturer and, as part of our evaluation report, disseminate his recommendations for treating the potential problem. After evaluation of the units individually, we assemble a representative group into a simple operating assembly, a code generator for instance, and evaluate their performance in an operating system. We are also establishing data exchange with some systems manufacturers and ultimately we should have a very valuable store of operating data on microelectronic elements.

Another important part of our "service after the sale" is consultation with organizations holding systems development contracts and applying the combined knowledge of both organizations in the selection of vendors and insuring that contract requirements pertaining to microelectronics are met. While some of our work will represent a decreasing effort with time, any slack thus obtained will be taken up by an increasing workload in this area.

The results of the evaluation program are of benefit not only to contractors and potential contractors, but also to the Center. Currently, within our group, we are studying the application of microelectronics to portions of the CONDOR missile; acting more or less as a subcontractor to our Control and Guidance Division. This particular application requires digital functions that will operate at a bit rate of 3 MC. and, when our evaluations show us devices that will operate suitably at this rate, we will incorporate them into the system and determine their compatibility with the rest of the circuitry. We have also designed and developed a UHF receiver that will be used as a vehicle for microminiaturization. At the present time, it is of conventional construction and portions of it will be microminiaturized as we obtain suitable hardware. Currently we are investigating a thin film I.F. amplifier that appears suitable. The particular amplifier is a relatively broad band device and requires the use of an additional resonant filter to obtain the desired selectivity. In this case our experience in the application of ferroelectric ceramic filters has been of great benefit and we are combining the ceramic filters with the thin film amplifiers. One of our technicians has devised a technique for mounting these elements in transistor cases and at present, using three filters in a TO-18 can, we can build 4.3 MC. filters with a bandwidth of approximately 100kc and a 60/6 db skirt ratio of 2:1. We feel that microminiaturization of the audio and a.g.c. portions will be relatively simple. In fact, we have hardware on hand that appears to be suitable. The greatest difficulty will be in the 246 MC, r.f. portions. We may ultimately be able to thin-film portions of the circuitry, but the high Q resonant elements will continue to be a problem.

One deterrent to the application of microelectronics has been the lack of documentation. Not only has there been no electrical standardization, but there has been no standardization of the physical attributes; package sizes and shapes, environmental requirements, etc.

Because of this we have prepared a Naval Air Development Center Specification, EL5-13, that provides some requirements and guidelines for both the manufacturer and user of microelectronic elements. The specification was written around the Proposed Navy Guide to Microelectronic Standards and, in the first amendment to the A revision, dated 10 July 1962, possesses a degree of sophistication, but still has deficiencies; particularly in reliability assurance procedures and interconnection methods. We have scheduled the specification for revision in the Spring of 1963, however, and hope that by that time we will have enough information to fill these gaps. In the meantime, and until such time as formal procedures are established, EL5-13 will be used as the basis for informal certification of sources of supply for microelectronic hardware. If the results of our initial evaluation indicates that the particular units are of a usable type and appear to be of generally high quality, certification action will be initiated based on the following:

1. Electrical performance in compliance with the manufacturers published data under a combination of load and temperature conditions.
2. Conformance with the general requirements of Specification EL5-13. Tests in accordance with MIL-S-19500, however, will usually be acceptable due to the generally more severe requirements.
3. Conformance with the reliability requirements of EL5-13.

The Naval Air Development Center will perform all electrical tests, but manufacturers certified test data will be accepted for environmental and reliability tests. We will ultimately stock quantities of certificated units for loan to systems manufacturers for preliminary evaluation.

We feel that our program in microelectronics is being effective in expediting the application of microelectronics to avionics systems and that, due to the efforts of ourselves and the other BuWeps activities, we will soon see the benefits of microelectronics in systems in the fleet.

THIN FILM MICROMINIATURIZATION AT NAVAIRDEVCEN

P. N. Drautman
U.S. Naval Air Development Center
Johnsville, Pennsylvania

When the thin film approach was chosen as the in-house effort in microelectronics for NAVAIRDEVCEN, this decision was the result of considerable thought, not only as to the ultimate results of such a program and the state of the industry but the availability of personnel and the equipment necessary to sustain the effort at the development level.

Two major steps were to be taken in order to acquire this basic capability: (1) The establishment of a suitable laboratory facility and (2) An R&D contract with General Electric Company in Syracuse, New York. In the former, we have achieved partial success in that we have succeeded in training two physicists and one senior technician, lacking in any previous experience in this field, in various aspects of the program. In this, we have had assistance from the GE Company calling very frequently upon their personnel and most especially upon their equipment.

The GE contract, which was concluded on 1 July 1962, had as its primary objectives, the development of high value capacitors and manufacture of certain specific thin film circuits. This work will be described by Dr. Hal Katz, of the General Electric Company, in a paper to be presented tomorrow.

In our in-house program, we feel that we have satisfied to the degree within our limit, two of our primary objects: (a) the establishment of a basic capability, and (b) application of techniques within the state-of-the-art. The next phase, R&D in thin-film microelectronic circuits, has not been undertaken and will not be until the installation of new equipment and the new laboratory is completed.

For those of you who have not visited NAVAIRDEVCEN or did not hear Mr. Martin's summary last year of our facility, I shall briefly repeat what we have been doing. In use we have one obsolescent RCA evaporator. It originally attained a vacuum of 10^{-3} Torr. By using D-C 704 fluid, removing some resistors from the line, and boosting the thermostat, we have been able to increase its initial performance by an order of magnitude. This unit had been further modified by the addition of two 200 amp. filament power supplies. Initially, one 50 amp. filament supply was all that was available. The location of the diffusion pump and general interior design is such that a cold trap cannot be effectively introduced.

This unit was to be replaced in October of 1961 by an electron beam vacuum system manufactured by Elion Instrument Inc. This system is designed to attain a vacuum of 5×10^{-7} Torr in 15 minutes. It was delivered in June 1962 and will be installed when the new laboratory is complete.

We have been able to formulate techniques following general thin-film procedures and to achieve fairly consistent results with thin-film conductors, resistors and capacitors. We have not, as yet, done any work with inductors. Experimentation with new materials and procedures will be conducted when the new laboratory is completed.

Although we have done some work on ceramic substrates, we primarily use glass microslides, and at the present, clean them with alconox, degrease them with isopropyl alcohol and a glow discharge. This simplified cleaning procedure has been adapted since our present location is in a rather dusty area. Ultimately, our cleaning cycle will consist of an ultrasonic cycle (detergent - super NZL - rinse - continuous degreasing in isopropyl alcohol until placed in bell jar, bake out at 250°C at 10^{-5}mm and glow discharge after introducing argon into the system). Just as there is no need to dwell on theoretical aspects of thin film formation, there is certainly no need to reemphasize the importance of cleanliness in the process since it contributes so directly to film formation.

On our unit, source temperature proved difficult to control so we have relied on variation of source distances and configurations in determining film properties. Studies of the effect of rate on deposition, temperature of the substrate, as well as time and the previously mentioned factors contribute directly to the mobility of atoms impinging on the substrate surface and the subsequent nucleation.

Experimenting with and gaining experience in the control of these parameters has occupied much of the past year. We are basically interested in materials, and, with the implementation of the electron beam unit, will be able to include refractory metals and dielectrics that are beyond our capability at this time. We have spent considerable time and effort in the production of conductive films of Sn, Pb, Cu, Au, Ag, Cr, etc. They have been interesting and informative from two points of view: (a) in the deposition of the metallic film where we have attempted to control various parameters, such as thickness, resistance, etc., and (b) in attaching leads. For the latter, we have employed standard soldering techniques, substitution of indium solder, and a form of TC bonding - where using a 25 watt Ungar imperial iron we attach 2 mil gold wire to aluminum films using no solder. The latter is a matter of technique in gauging the pressure, heat control and absolute film cleanliness.

We have done many single films and crossed film cryotron units for the Surveillance and Reconnaissance Division of AEEL. Initially, we deposited a six unit, five layer, cryogenic flip-flop but the finished product proved too sophisticated for the test methods then available and considerable effort was devoted to producing films which became superconductive at the proper temperature. The transition temperature of tin, which initially presented a problem proved to be dependent on internal stresses created at the time of deposition due to the difference in coefficients of expansion between film and substrate. This is noted in the Handbuch der Physik, v. 14 for anyone interested in pursuing this further. Caswell, Priest and Budo of IBM further reported on these effects at the Thin Film Conference recently held in Glenwood Springs, Colorado. An interesting study of aging of thin films was carried out unexpectedly and informally. While setting up a VIP demonstration, it was necessary, due to lack of time to prepare new samples, to use a film which had been stored for three months. No change in switching characteristics was found.

In depositing most circuit cryotron units, the problem of attaching leads was solved by initially depositing lands of Cr-Au, Cr-Cu, and making connections directly to them. A two source evaporation technique was employed in which a thin layer of Cr was deposited, the Au or Cu evaporation begun and the Cr discontinued. Effectively, this becomes a three layer deposition, Cr, Cr-Au, Au, with the connection made to the latter.

We have attempted an evaluation of ultrasonic welding in that we submitted three groups of seven thin film samples each, Nichrome, Sn, Pb, Au, Ag, Cr, Al to a commercial company for ultrasonic welding with leads of Al, Au, and Cu to be used in each group respectively. The results were extremely disappointing and until new equipment is installed, we will continue to employ manual TC bonding and soldering with extreme cleanliness and care. Leads of aluminum foil clipped to the film have also proved useful in making rapid tests to determine whether a group of films obtained in a certain way will be of interest for more detailed studies.

Nichrome resistors have been deposited. The best values consistently obtained are 200-250 ohms/sq.

Cermets have been attempted, initially making use of SiO and Cr. The range covered was 100-300 ohms/sq. No real control of the mixture is available on the present evaporation apparatus. Better results should be obtained with the new equipment.

Considerable effort has been devoted to capacitors, and we feel that we have achieved some measure of success in this area. Basically, capacitors should have low dissipation factor, a low leakage current, high dielectric strength and small temperature changes of capacitance. It is difficult to produce a device incorporating all features. We have made two types using Al, a dielectric layer of SiO measuring approximately 5,000 A and a counter electrode of Al. Capacitors of this type were generally of low capacitance per unit area but capable of operating at high frequencies. We have recently been concentrating on the anodized Al dielectric which gives us better control and a thinner non-porous dielectric film thereby increasing our capacitance. Using aluminum as base layers and counter-electrodes and aluminum oxide as the dielectric, capacitors have been made ranging from approximately 0.18 - 1.63 mf/in^2 corresponding to D.C. forming voltages of 230 and 20 volts. The dielectric constant was determined to be approximately 8.4 ± 15%. The reproducibility of D.C. formed aluminum oxide capacitors is good because oxide thickness can be accurately controlled. The thickness is primarily a function of the forming voltage and the oxide forms at a constant rate. Using the anodizing techniques of Hass* it is assumed that approximately 13A/V is formed for two minute anodization. We have not been able to accurately measure oxide thickness by optical methods although a technique is currently under development. The above capacitance values may be somewhat high compared to their forming voltages due to some diffusion of the counterelectrode into the oxide layer. Using an anodizing bath of 3% ammonium tartrate (pH = 5.5) we get a barrier type, non-porous oxide layer. This type of oxide layer should prevent the counter-electrode from diffusing more than one or two molecular layers. We have experimented with Au as counter-electrode but find it offers no advantage at the present time.

Capacitor characteristics such as dissipation factor, leakage current, insulation resistance, breakdown voltage, etc., as well as environmental behavior of operating capacitors are being evaluated at the present time.

About all that can be said at the present is that leakage currents are very low, and breakdown voltages are not too consistent, with some as high as 50 to 60% of the forming voltage. We are experimenting with A.C. anodizing of aluminum films but have no results to report at this time.

*On the Preparation of Hard Oxide Films with Precisely Controlled Thickness on Evaporated Aluminum Mirrors" by George Hass, J. Op. Soc. Am., Vol. 39, No. 7, July 1949.

We have been working with three-layer squares in two sizes approximately 1/10" and 1/4" on a side. Some typical capacitance values are given below:

Approx. 1/10" AL-AL				Approx. 1/4" AL-AL			
F.V. (VDC)	Capacitance (µµf)	Area (in^2)	µf/in^2	F.V. (VDC)	Capacitance (µµf)	Area (in^2)	µf/in^2
50	14,000	0.016	0.87	20	129,000	0.079	1.63
70	9,600	0.017	0.56	30	92,500	0.080	1.17
90	7,900	0.015	0.53	40	75,000	0.081	0.93
110	6,260	0.015	0.41	50	57,200	0.078	0.73
130	5,000	0.014	0.36	60	50,200	0.081	0.62
150	3,850	0.013	0.30	70	42,200	0.078	0.54
170	4,300	0.017	0.26				
200	3,700	0.016	0.22				

We have been making our own masks. Here we have taken advantage of our poor vacuum since at the best vacuum we can attain, brass masks are still usable and, of course, brass is easily etched and more readily controllable than most materials. We have briefly and spasmodically initiated programs to produce our own stainless and molybdenum masks, but at the present time, lack the personnel and working space to successfully complete a program in etching masks to close tolerances. Realizing our limitations in this area, we have attempted to evaluate masks commercially available.

Unfortunately, in spite of positive advertisement, they generally prove to be not too available, and those etched commercially have proved to be, in most instances, inferior or at best no better than our own. Two other methods, including electron beam burning have not proved too successful to date.

We are presently employing a Zeiss Interference Microscope for all thickness measurements. A Zeiss 35 mm. contax camera is used for white light and Thallium Light Photographs. The Zeiss was chosen on the basis of accuracy of measurement, range of thicknesses measurable, and overall versatility of the instrument. Whereas the standard type Interferometer is comparable in accuracy, it does not have the capabilities of the Zeiss. The Zeiss can magnify images up to 480 times, thus rendering thin-film surface studies possible. A rough estimation of film thickness is made by direct observation of band displacement, and band correlation is achieved by observation with white light. More exact measurement is accomplished with Thallium light. It can measure in the depth range of from 0.03 microns to about 2 microns, and its estimated accuracy is approximately 10%. Increased accuracy of the Zeiss is expected as the amount of external vibration is reduced with permanent location.

Using Kodak Panatomic-X, black and white film, a series of test rolls were exposed to various gold-on-chrome-on-glass edges and nickel films. Brightness control and aperture diaphragm settings were held constant, and the same objective power and mirror reflectivity were used throughout the experiment to determine optimum exposure times for both white and Thallium light. Simultaneously, optimum developing and printing conditions were found with the cooperation of the Photographic Laboratory. Optimization of band spread vs. sharpness of focus was attempted and it was found within a reasonable degree of accuracy. It should be noted that focusing and measurements will vary with the eyesight of the observer.

Although satisfied with results, we realize limitations and still seek better methods. A study of surface characteristics, for example, contours and graininess of thin film surfaces, is presently being initiated; and a feasibility study is being made on a vibrating crystal method for monitoring the deposition rate of our vacuum deposited thin films. Briefly, the substance being evaporated would be allowed to deposit on the resonating crystal face. The increased thickness causes the resonant frequency to decrease. Measuring the frequency as it decreases provides a method of determining film thickness during evaporation. The solid state microelectronics group at General Electric, Syracuse, New York has developed such a device. Other methods for rate monitoring and thickness measurement are being investigated.

I have dwelt rather extensively on our limitations but I did not wish to convey the impression that we have not kept astride of thin film developments. In addition to our own work we are fortunate to be in communication with the outstanding thin film groups in the

United States and therefore have an excellent index of industry's capabilities in thin film microelectronics. Actually, we have been more or less "strengthened by adversity", dismantling and reassembling pumps, changing oil, constructing new power supplies, etc., has given us a real appreciation of the basic practical problems. If we had started with shiny new equipment we might never have seen the inside of a diffusion pump and would be inclined to take too much for granted.

In conclusion, I would like to outline just what our frequently referred to new laboratory will be like. I feel rather like Cinderella at the moment. We are moving from the corner of another lab to a 40' by 40' area of our own. Forty feet by 16 feet of this space will be Class IV Clean Room area and most of our operating equipment will be in there. The Clean Room Facility is of modular construction and is being supplied by Shielding Inc., Riverton, New Jersey. Of the remaining 40 x 24 area, one section, 20 by 24 feet will be General Laboratory area containing chemical work tables, a hood, our RCA evaporator, and a new sputtering system which we have started assembling at the present time.

The remaining area is divided in half - one part being desk space, the remainder will contain the analytical balance, Zeiss interference microscope, regular microscopes and measuring equipment.

In addition to the Elion unit previously mentioned, we will have a second vacuum deposition system manufactured by Bondee. An electron bombardment unit by MRC will also be in this area. Additional equipment will include a new pyrometer, and a K&S TC bonding unit, Model #410, Vacuum gauge check unit and a CEC Leak Detector.

We have spent a great amount of time and thought in ordering and writing specifications for our new equipment and in its arrangement in the new laboratory. We are very fortunate in having a tremendously interested group; all of us having suffered through innumerable small crises that arise, and are looking forward to our new equipment and laboratory. We feel that we have developed into an efficient group and with the establishment of this new laboratory, expect to offer more significant information at the next meeting of this group.

NAFI LABORATORY PROGRESS REPORT ON MICROELECTRONICS

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During the past three years an abundance of review and survey reports on microelectronics has appeared in the scientific and popular press. This plethora of publicity has led to confusion. However Fortune magazine gives a hint of the true state of affairs regarding thin-film microelectronics. The author says that: "The development of thin films, as it stands today, is in some respects a throwback to the days of trial-and-error Edisonian invention. Lacking a thorough understanding of all the basic physical properties of thin films, engineers are forced to rely on empirical recipes for making them. Because conditions vary from one laboratory to another, two men following essentially the same procedure often produce films that perform quite differently.

"This confusing state of affairs is due in large measure to difficulties in scientific communications. Most technical journals have such a backlog of reports that they publish too slowly to keep abreast of developments, and besides, many of the techniques are jealously guarded proprietary secrets. Rumors are spreading to an extent not common in scientific circles. The field is permeated with a kind of hysteria that seems to grip most new and exciting technologies: at this stage, scientists and engineers are not always careful to distinguish between what they actually have done and what they hope to do." (1).

One of the functions of the NAFI laboratory is to make this distinction. This report briefly describes NAFI laboratory progress in the making of masks, substrates, conductors, resistors, capacitors and active components.

Masks

The successful production of thin-film microcircuits is strongly dependent upon the ability to deposit desired materials on accurately defined areas on a substrate. Hence, we are continually investigating new methods for improving our mask making techniques.

Our masks are made by a photo-etching technique. Three-mil thick stainless steel, AISI 304, is coated on both sides with Kodak Photo Resist (KPR); inserted in an envelope consisting of mirror-image film positives accurately registered; exposed to ultraviolet light, and spray etched in 43% ferric chloride solution,

Film alignment is difficult, hence we have developed a film alignment jig to facilitate this operation. The accuracy of registration of the KPR images, from one side of the mask to the other, will depend on the accuracy of alignment of the films. The location of one film is fixed, and the other is positioned accurately, by means of a crossfeed and rotary table. Alignment is determined visually, using a low power microscope.

In order to assure uniform etching of masks, we use a rotary etching rack (AV-3258). This rack, which is similar to the one in use at Lear, Incorporated, is a turntable which passes the stainless steel mask blanks in a vertical plane, equidistant, between the spray nozzles of a Centre Circuits, Model 201, etching machine. The rotary motion improves the uniformity of etching. The mask blanks have KPR images affixed. The etchant is 43% $FeCl_3$.

Masks, etched from 3-mil stock, are adequate for defining conductor lines, pads, and capacitor electrodes. However they are too coarse for defining certain resistor patterns. Some improvement can be attained by etching resistor masks from 1-mil stock and supporting this mask with a much thicker, coarse-patterned mask. Where the utmost in accuracy is required, expendable masks of evaporated copper are used.

Substrates

The integrity of a vacuum evaporated thin-film circuit is influenced by the mechanical, chemical, thermal, and electrical properties of the substrate material and the condition of the substrate surface.

At present we are evaporating circuits onto Pyrex glass substrates coated with SiO about 10000A thick. Evaporated silicon monoxide, because of its low surface mobility, smooths out minor surface defects and acts as a barrier to surface alkali ions (2).

Although glass has many properties that make it attractive as a substrate for microcircuits, its heat conductivity is low. Also, its mechanical strength leaves something to be desired. Because of these deficiencies we are investigating other substrate materials. In general, ceramics excel glass in heat conductivity, mechanical strength, and high temperature capabilities. Among ceramics of interest are high alumina (96% Al_2O_3), high beryllia (96% BeO), Fotoceram and

Fotoform. The latter two are of unique interest because precise intricate holes or slots can be formed in them by a proprietary photochemical process. However, Fotoceram and Fotoform are proprietary (Corning Glass Co.) materials, and hence their universal adoption for microelectronic applications is unlikely.

Alumina and beryllia have many properties that make them attractive as substrates for microelectronics. They have good overall thermal, electrical, chemical, and mechanical properties. High beryllia ceramics possess all the desirable properties of the aluminas with respect to electrical, chemical, and mechanical characteristics, but also have a thermal conductivity approaching that of aluminum metal. Beryllium oxide, however, is toxic. When in powdered form and in a condition which allows it to be taken into the lungs, beryllia can be a dangerous poison. However, beryllia in the form of ceramic substrates for microcircuit applications probably presents no health hazard. Beryllia may very well prove to be the preferred material for microcircuit substrates.

At present we are evaluating alumina materials rather than beryllia. This choice was made because of the high cost of beryllia rather than because of its latent toxicity. The chief objection to the use of ceramics for microcircuit applications is surface roughness which cuts down on the yield of evaporated capacitors. Any manufacturing or surface treatment techniques which would improve the alumina product would probably be applicable to beryllia.

We are encouraged by the cooperation we are receiving from manufacturers of ceramic materials. Diamonite Products Manufacturing Company has submitted samples of a particularly fine-grained alumina with a surface finish between 4 and 6 microinch RMS. Because of the inherent crystallinity of alumina ceramics this surface finish probably represents the ultimate for mechanically polished material. The surface is still too rough for depositing short-free capacitors. It can be materially improved by the deposition thereon of a layer of silicon monoxide 15,000A thick. The improvement attained is not sufficient because of too high density of remaining pits which cause shorts in evaporated capacitors.

For this reason we are confining our substrate investigations to glazed ceramics. The normal commercial product contains ripples which cause poor definition of circuit patterns evaporated through metal masks. Recently, producers of glazed ceramics have made an effort to produce a product suitable for use as substrates for microcircuits. Among the better materials currently under study in our laboratory is the Americal Lava Corporation product, designated Alsimag 614, coated on one side with their special glaze #743. The glaze is basically a lead-boro-silicate glass with approximately 3% alkali content. It has a low dielectric loss and a high surface resistivity under conditions of high humidity. The softening temperature is approximately 725°C; however it can be used at temperatures up to 700°C in vacuum or in oxidizing atmospheres without damage to the surface. A surface finish of better than 1 microinch RMS is recorded on surfaces of this type.

Substrate Cleaning

The quality of an evaporated film is strongly influenced by the condition of the substrate surface. The substrate surface should be examined visually in collimated light for pits, scratches, and other defects which could cause pinholes in evaporated films. The acceptable substrates should then be thoroughly cleaned to remove all traces of oily deposits. There are probably as many different acceptable cleaning procedures as there are technicians working in this field. The cleaning procedure that we use is outlined below:

1. Rinse in tap water to remove loose dirt.
2. Scrub in 3% solution of Alconox in tap water, using high grade absorbent cotton as a scrubbing pad. (Add precipitated chalk if necessary.)
3. Rinse in tap water.
4. Ultrasonically clean in 3% Alconox solution for 15 minutes.
5. Rinse in tap water.
6. Ultrasonically clean in distilled water for 10 minutes.
7. Ultrasonically clean in ethyl alcohol for 10 minutes.

The substrates are then placed in a previously cleaned mask-substrate holder assembly. The loaded assembly is immersed, mask-side down, in isopropyl alcohol vapor. The unit is then slowly withdrawn and, while still hot, placed in the evaporator.

Although a number of tests have been proposed for evaluating the cleaning procedure, only performance tests are valid. We evaporate (3000A) aluminum on the substrate, then anodize (3) at 100 volts (1270A) in 3% tartaric acid (pH 5.5 with NH_4OH), and then inspect the substrate visually for evidence of spalling.

Conductors

Evaporated aluminum films or composite films of chromium - chromium copper - copper or chromium - chromium gold - gold, are frequently used as conductor lines and pads in thin-film microcircuitry.

Composite films for conductors are not easy to deposit in a reproducible manner. Control is a problem. An alloy of the two components of a composite film is suggested as source material. One component to secure adhesion to the substrate and the other to present a solderable or bondable surface. To insure preferential evaporation, the adhesive component should have a higher vapor pressure than the solderable component at any given temperature. Vapor pressure information on metals that are suitable for such alloys are given in Table I. Chromium and titanium are omitted because they do not vaporize at sufficiently low temperature. Lead and magnesium are omitted because they vaporize at too low temperatures.

Table I.

Approximate Melting Points and Temperatures Associated With a Vapor Pressure of 10^{-5} torr for Selected Materials

Metal	Temperature (°C) at which vapor pressure is 10^{-5} torr	Melting Point
*Mn	650	1260
Ag	750	960
*Al	875	670
*Be	875	1275
Cu	925	1080
Au	975	1060

*Metals that adhere well to glass

An examination of Table I indicates that Mn-Ag, Mn-Cu, Mn-Au, Al-Cu, Al-Au, Be-Cu, and Be-Au are alloys that may be used as starting materials for evaporating solderable lands. The adhesion and soldering properties of these alloys in various ratios have been studied by several investigators. Be-Cu and Mn-Ag alloys are reported to have favorable properties.

We have been unable to produce evaporated binary alloy films which have the combined characteristics of adhesion and solderability (or bondability) possessed by such composite films as chromium-copper or chromium-gold. The alloy films may be adequate, but not optimum.

Studies on evaporated alloy films are being continued. If a suitable alloy can be developed, it is envisioned that conductor lines and pads can be deposited by evaporating a preweighed chunk or pellet from a single reusable evaporation source. Alloy pellets in a hopper could be fed to a preheated boat in an automated production process for depositing thin-film microcircuits.

If the leads of inserted components are to be attached to evaporated circuitry by thermo-compression bonding, aluminum appears to be a suitable material for conductive films. Even though aluminum films are protected by a hard adherent natural oxide coating, this oxide is readily penetrated during the thermo-compression process so that gold leads are firmly bonded. Gold-aluminum conductive films are of special interest because leads can be attached to them by either soft soldering or thermo-compression bonding.

Resistors

Resistors are the most widely used components in microelectronics. Hence, investigations of resistor film materials, their properties, and methods for their deposition, are of great importance. Characteristics in which resistor-film improvements are needed are these: reproducibility, thermal and electrical stability, resistance per square, and ability to withstand high temperature environment.

During the past year our experiences with evaporated thin-film resistors has been limited to chromium-silicon monoxide cermets. The cermet formulas are those suggested by IBM in their quarterly reports on Contract #163-9142(X). The constituents of the cermets are chromium of 99.8% purity and particle size between 325 and 400 mesh, vacuum degassed silicon monoxide of the same particle size, and colloidal silica sold under the trade name Cab-O-Sil. The mixture for resistors having resistance up to 250 ohms per square consists of 70 atomic percent chromium and 30 atomic percent silicon monoxide. Five-tenths percent by weight of colloidal silica is added to the mixture to prevent agglomeration and assure even flow down the feeder chute. The constituents must be thoroughly mixed prior to evaporation.

Since the constituents have different vapor pressures, flash evaporation is used. This method assures the instantaneous evaporation of all the constituents.

The evaporation source is a tungsten ribbon about an inch wide and two inches long, heated to about 1800°C. The pre-mixed powder is fed to the hot ribbon by a worm driven powder feed and metal chute. The chute is positioned above and a short distance to the side of the evaporation source. This arrangement permits the cermet powder to fall on the middle of the hot ribbon and keeps the feed mechanism from shadowing the substrates.

During the evaporation cycle the substrates are heated to 220°C and the evaporation pressure is 5×10^{-5} to 1×10^{-4} torr. Evaporation is stopped when the value of the monitored resistor is about 1.3 times the required final value. For example, if a resistor is to have a final value of 250 ohms per square, evaporation is stopped when the monitor slide resistance is about 325 ohms per square.

The resistor is adjusted to its final value by an annealing process. But before it is annealed it is protected by a film of SiO. The substrate temperature is maintained at 200°C in a vacuum of 5×10^{-6} torr while a silicon monoxide film 10,000A thick is evaporated at a rate of 20A per second. The resistor is baked in a reducing atmosphere (forming gas: 5% H_2 and 95% A) until the desired resistance value is attained. A temperature coefficient of resistance of -50 ppm/°C must be taken into account when setting the anneal stop value. The annealing time may take from two to four hours.

The resulting resistors have many desirable properties, including ruggedness and long term electrical stability.

We have evaporated satisfactory cermet resistor films having resistances up to 600 ohms per square. The latter films were made from a cermet mixture containing 65 atomic percent chromium, 35 atomic percent of silicon monoxide and 0.5 percent colloidal silica. The temperature coefficient of resistance of these resistors may be as high as -150 ppm/°C.

The fabrication of cermet resistors presents some problems. Although the cermet particles are larger than 400 mesh, they are fine enough to be dispersed by the vapor stream emitted by the evaporation source. Fine cermet particles eventually cover the walls and permeate every crack and crevice in the evaporator. The particles may contaminate the vacuum gauge tube. Also, fine SiO particles, being somewhat hygroscopic, absorb moisture which degrades the vacuum after a few coating cycles unless the evaporator is frequently cleaned. These difficulties with cermet evaporation, which are prevalent in the customary bell jar evaporator, may be absent in the IBM production coater. In this coater the evaporation sources are in semi-isolated chambers where baffles may be effectively placed.

We have found that the thickness distribution of cermet films shows a departure from that predicted by Knudsen's cosine law. Also, the distribution varies from batch to batch. Interference between the stream of cermet powder fed to the evaporation source and the vapor stream emitted therefrom is suspected. No solution to this problem is immediately apparent. Perhaps a refinement of the powder feed geometry and the evaporation source geometry is needed.

It is desirable that all resistors made during an evaporation cycle show very nearly identical resistances per square so that they can be annealed simultaneously. Resistor films uniform within 1% over substrate areas up to 30 sq. in. are deposited in a single cycle in one of our 18" diameter evaporators. The high degree of uniformity of coatings is assured by the compound circular motion described by the substrates during an evaporation cycle. The substrate wafers are mounted in individual holders attached to one of four circular plates mounted in a horizontal plane on a revolving wheel. Thus, the substrates describe epicyclical paths during a coating cycle. The wheel revolves 60 times per minute while the plates rotate from one to four times, depending on gear ratio used, during a revolution. The evaporation source, or sources, are located directly below the circumference of the outermost circle described by the rotating mechanisms. Theoretically, the greatest degree of uniformity of coating is achieved when the distance from the evaporation source to the plane of the substrates is equal to the radius of the outer circle. In practice, it was found more desirable to locate the evaporation sources at a greater distance. The choice of distance is selected as a compromise between depositing films rapidly and minimizing shadowing effects of the masks at large angles. Monitoring resistance values presents no serious problem if the evaporation source is not too directional. Normally the resistance monitor slide is mounted in the center and in the same plane as the substrates. If the resistance of the monitor slide does not correspond with the resistance per square of the samples, compensation can be made by raising or lowering the monitor slide or by changing its length to width aspect ratio.

In a coating arrangement constructed as described above, the evaporation sources are displaced about the circumference of a relatively large circle. Each source contributes to the deposition of a uniform film on all the substrates. Hence, more than one source can be used to increase the speed of deposition, or two or more sources can be used for the codeposition of two or more materials. Also, different types of evaporation-source heaters such as resistance, electron bombardment, and induction, can be operated simultaneously, or individually, in the evaporation chamber.

This coating arrangement is also superior for the deposition of silicon monoxide films. Silicon monoxide films deposited on the moving substrates have a much lower density of pinholes than those deposited on stationary substrates. The vapor stream, striking the substrate at varying incident angles, apparently fills the incipient pinholes.

There are some undesirable features of this evaporator:

1. It does not permit mask changing during a coating cycle.

2. It does not allow for precise monitoring of substrate temperatures.

These objections are not serious where batch coating can be used and where substrate temperature is not critical.

Capacitors

Capacitors can be formed in place on a smooth insulating surface by the alternate deposition of metals and dielectrics. A capacitor of the simplest structure consists of two metal electrodes separated by a dielectric layer. The capacitance of such a structure can be increased by making the dielectric layer thinner, increasing the number of metal-dielectric layers, or by using a dielectric having a higher dielectric constant.

We have experimented with evaporated titanates and titanium oxides as capacitor dielectrics. Films having reproducible properties were found to be extremely difficult to produce with present coating equipment. Experiments with these materials will continue after our present equipment is updated.

We are taking a second look at SiO as capacitor dielectric. The optimum value of the dielectric strength of SiO is claimed (4) to be about 2 x 10^6 volts/cm as compared to 2 x 10^5 volts/cm for mica. This means that an SiO film 1500A thick will not break down at less than 30 volts. Or, SiO film 3000A thick should withstand an electric field of 30 volts with adequate margin of safety. Normally, an film 20,000A thick would be recommended for insulating 30 volts. If the inherent dielectric strength of SiO could be realized in practice, it would be an important accomplishment. Pinholes cause failure in SiO films used for insulation at voltages less than their dielectric strength. Hence, means must be sought to either prevent or to seal pinholes. Our studies indicate that the pinhole problem can be considerably reduced if certain procedures are adopted. First, the substrates should be carefully selected as to surface condition. Substrates whose surfaces contain pits, scratches or other visible imperfections, should be rejected. The surfaces of the of the acceptable substrates should be thoroughly cleaned, and coated with an evaporated film of silicon monoxide about 10,000A thick.

The metal of the bottom electrode should be one which shows excellent adhesion to silicon monoxide; has high electrical conductivity; and is capable of being vacuum deposited in layers at least 4000A thick and still have a mirror finish. In other words, aluminum is the preferred metal for the bottom electrode of an evaporated metal-SiO-metal capacitor.

All of the evaporation operations should be conducted with care. The quality of evaporated films is influenced by evaporation conditions. Silicon monoxide films, evaporated under conditions which yield films having a dielectric constant of about 6.0, are superior for capacitor and insulator applications. Such films are deposited at about 20A/sec at a pressure of 5 x 10^{-5} torr.

Pinholes in SiO films are frequently caused by "spitting" from the evaporation source. We have tried out several different sources, including the Drumheller "chimney" evaporator and a baffled source sometimes called the Clark evaporator. Unless precautions are taken to avoid too rapid heating, the chimney evaporator spits. The baffled evaporator emits a clean vapor stream but frequently becomes clogged because vaporized SiO condenses on the cooler parts of the lid in the vicinity of the aperture. We have combined the desirable (and also, some of the less desirable) features of the two sources in a hybrid version. We have installed a chimney in a baffled source. Sufficient heat is generated by the chimney to minimize condensation of SiO on the baffle and lid. This source is not as efficient as the parent versions.

The probability of pinholes occuring in evaporated silicon monoxide films can be reduced by evaporating onto a moving substrate as mentioned previously.

If silicon monoxide is deposited on an aluminized substrate, pinholes can be sealed by anodizing, in an ammonium tartrate bath.

Pinholes in dielectric films can be sealed with high resistivity silicon. Evaporated silicon behaves like a metal in that it has a tendency to diffuse over the surface of freshly evaporated SiO and fill the pinholes. The resistance of the silicon "shorts" in the silicon monoxide film is too high to adversely affect the electrical properties of the layer.

A similar technique for filling pinholes employs evaporated aluminum instead of silicon. When this procedure is used, the silicon monoxide is applied in two or more steps. For example: To produce a 3000A thick film, a layer of silicon monoxide, 1500A thick, is deposited, followed by a layer of evaporated aluminum 50A thick. The aluminum is evaporated at about 5 x 10^{-6} torr. The aluminum layer is subsequently oxidized by bleeding oxygen into the system to increase the pressure to 10^{-3} torr. Then, after about five minutes, the system is reevacuated to about 5 x 10^{-6} torr and the film then built up to the desired thickness with silicon monoxide.

Active Components

Evaporated thin-film microelectronics will probably not gain complete acceptance by industry until active as well as passive components can be deposited by compatible techniques.

The fabrication of conventional Ge and Si diodes and transistors in thin-film form has been a subject of investigations in many laboratories. In order to achieve transistor action in a semiconductor film, the deposited material must be in single crystal form. Also, extremely small and well defined regions of the film must be doped to show specified resistivities of the required "p" or "n" type.

Single crystal films can be grown epitaxially on single crystal substrates. Proper annealing treatment of thin-films of some materials evaporated onto the surfaces of single crystals causes the film to assume the crystal habit of the underlying crystal. But we are interested in evaporating *active* elements on *passive* substrates.

A literature search indicates that the Sylvania Microelectronic Laboratory claims to be able to deposit single crystal active devices on ceramic substrates. The techniques are proprietary and they will only say that the process involves an "epitaxial technique on a ceramic substrate with special surface treatment but with no single seed on the base" (5). Since details for fabricating these single crystal devices is not available, we are seeking other solutions to the problem of fabricating thin-film active components.

We learn that several laboratories are investigating methods for fabricating active devices that are quite unlike conventional transistors but which are expected to be capable of performing some of the same functions. The active material in many of these proposed devices is a semiconductor having a relatively large energy gap. Sometimes these devices are referred to as "dielectric" as opposed to "semiconductor" devices of which the conventional transistor is an example. Thin-film active devices of the dielectric type offer the following possible advantages over semiconductor devices:

1. Greater resistance to radiation damage
2. No semiconductor surface problems
3. Inherent high frequency capability
4. Compatibility with thin-film integrated circuitry
5. Ease of fabrication

Some of the thin-film semiconductor and dielectric active devices currently under investigation include: thin-film selenium diodes at General Electric; metal interface amplifiers (MIA) at Philco and Raytheon; tunneling devices at California Institute of Technology and Electro-Optical Systems; titanium tunnel diode at Republic Aviation; thin-film tunnel diode at Texas Instruments; space-charge-limited-current diode and triode at the University of Birmingham (England); and the thin-film transistor (TFT) (6). These appeal to us as offering interesting potentialities. These devices incorporate cadmium sulfide as the "active" material. Accordingly, we are investigating a technique for depositing CdS films and studying the structure and properties of the deposited films.

Cadmium sulfide, as starting material for dielectric active electronic devices, occupies a role comparable to that of germanium in the development of conventional transistors. It may not represent the ultimate material but it is the best available. Cadmium sulfide, like most other compounds, dissociates somewhat when heated to its vaporizing temperature. The higher the temperature, the greater the dissociation. If cadmium sulfide is heated only a few tens of degrees above its vaporizing temperature, the resulting films are dark. This indicates an excess of cadmium. Evaporation from a metal boat yields discolored films because of strong local heating. We have achieved best results by evaporating CdS from a silica crucible. A flat tungsten spiral filament serves as the heating element. It is in close proximity with the powered cadmium sulfide. The filament temperature is controlled by an autotransformer. The pressure in the coater was 1×10^{-5} torr to 5×10^{-6} torr.

The temperature of the substrate may have a profound influence on the stoichiometric properties of evaporated CdS films. If the substrate temperature is too high, the films are dark, indicating an excess of Cd. We have found that the substrate temperature should range from 100°C to 200°C. In this range of temperatures the dissociated elements apparently recombine to form nearly stoichiometric CdS characterized by its lemon-yellow color and high resistivity.

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MICROELECTRONICS PROGRESS REPORT

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At the last Microelectronics Meeting the Naval Ordnance Laboratory reported on its interests and plans for exploratory research to develop new components and to utilize new physical phenomena for weapon functions. In keeping with the specialized mission of today's Conference, our present report will concern itself with those phases of our program which may ultimately result in microelectronic functional components or systems. The program will be reported in two phases; basic research in thin films, and advanced engineering in microelectronic circuitry and devices.

BASIC RESEARCH

Thin Semiconductor Films - For the past several years, there has been increasing interest in producing thin semiconducting films which are strongly oriented with respect to their substrates. These films, hopefully, would be single crystal, chemically pure and sufficiently perfect physically to insure high mobility and reasonable lifetime. Films of this nature have been made and are the basis for the many epitaxial solid state devices currently available. One important drawback of present technology is that these films are put down on the same substrate material as the film itself. Thus, measurements of their electrical and optical properties are limited. In the past year, NOL has evolved techniques for producing single crystal or epitaxial films of PbS on NaCl crystals by vapor deposition. The quality of the films compares quite favorably with that of good quality natural galena. Carrier concentrations of 1-2x10^{18} electrons/cm^3 can be obtained regularly with mobilities over 400 cm^2/volt sec at room temperature and over 5000 at 77°K. So far measurements have only been made on films whose thickness ranges from 0.3 microns to 8 microns. No effect of thickness on any electrical or optical properties have been observed. X-ray data confirms the high degree of crystalline perfection in these films.

The possible applications of these thin films to microelectronic hardware are many and varied. While the lead salts are not well suited to transistor action, they can be used in esaki diodes, MIA's, unifunction devices and other solid state device functions. Additional studies on the fundamental properties of the lead salt epitaxial films on various substrates are currently under way. The application to device technology remains to be done.

Field Effect Modulation - One interesting accomplishment has been the discovery of an electrically modulated photodetector. There are two phenomena which have been well known for some time in semiconductor physics. First, the photoconductivity of a specimen depends on the depth of light penetration. The hole-electron pairs generated by the incident radiation recombine by either bulk states or surface centers depending on how strongly the radiation is absorbed. If the light is absorbed within 10^{-5} cm's of the surface, the recombination process would be dominated by the surface centers. The parameter describing this is the surface recombination velocity.

The second phenomena is the dependence of the surface recombination velocity on the surface barrier height. If there is a barrier at the surface for minority carriers, as an example, the recombination of excess carriers will be limited by the height of the barrier. The higher the barrier, the lower the recombination process.

Suppose we combine these two phenomena. By varying the surface barrier height, the recombination velocity can be varied in a controlled fashion. This variation, in turn, will modulate the photoconductivity of the semiconductor for strongly absorbed radiation. This phenomena can be applied to any photoconducting material which is subject to limitations by surface recombination processes. The net effect is to produce a modulated electrical signal which is proportional to the intensity of the incident radiation. Except for the degree of cut off, this is fully equivalent to having a chopper in front of a conventional photoconductive detector. Extremely high chopping rates are possible with such a device, e.g. chopping rates of less than a microsecond are possible on germanium and InSb intrinsic photodetectors. By combining this phenomena with thin film or functional block devices, extremely compact sensing elements are possible.

Magnetic Film Logic - Our previously reported studies of all magnetic logic systems utilizing domain wall motion in strained nickel-iron wire have been extended to thin films. An unusual property of strained high permeability magnetically saturated nickel-iron wire is that the field required for domain wall motion is considerably less than the field required for the creation of such a wall. A similar characteristic is observed in thin nickel-iron films which have been deposited in a strong magnetic field. Such films have been used to construct all magnetic shift registers and are the basis for our current magnetic film logic effort.

As in the case of the strained wire logic system, a thin film logic circuit would consist of the Ni-Fe film and a printed circuit for the signal currents all contained within a set of close-fitting solenoids which provide the field for switching the film. The signal current acts as a trigger to produce a domain wall which is then moved by the solenoid fields. The switching of the small amount of flux by the signal current thus controls the switching of a much larger area of the film and permits a power gain to be obtained in the circuit.

We are presently studying the performance of films prepared by chemical, electrochemical, and evaporation techniques to determine film characteristics best suited for logic circuits. One major problem is homogeneity wherein local discontinuities inhibit domain wall motion. A Kerr magneto-optic effect device is being constructed to observe the domain wall patterns produced by the switching fields and the location of film defects.

In order to expedite the development of suitable films, our Mr. Irons has accepted the invitation of Dr. Lawson of the Royal Radar Establishment to visit and work with them on the deposition of nickel-cobalt films on glass and metallic substrates. If suitable films can be produced, it should be possible to design all magnetic logic circuits that are reliable and easily fabricated.

ADVANCED ENGINEERING

Broad Objective - The goal of the NOL advanced engineering program is to bridge the gap between research in microelectronics and ordnance engineering. It is intended to develop in-house competence in the application of microelectronic techniques to ordnance, select one or more fabrication processes suitable for ordnance use, and introduce microelectronics into NOL-developed ordnance.

While it is expected that the microelectronic techniques eventually will provide more economical hardware, this advantage is not available today and probably will not be available in the very near future. This is particularly true for programs involving only small production quantities, which seem to be prevalent today. However, an advantage of microelectronics which can be utilized in the near future, is the small size or compactness of such devices. This permits much greater circuit sophistication per unit volume and should result in higher system performance.

Our approach is to develop more sophisticated circuits for use in already-compact ordnance devices and to evaluate for ordnance use the microelectronic fabrication techniques currently in use in industry and other government laboratories. At this time there is no in-house effort on constructing a microelectronic fabrication facility; all fabrication will be done on contract to industry, at least for the present.

One circuit being developed is a correlation detector for detecting sinusoidal signals in the presence of noise and interfering signals. The principles employed are not new, but they are, nonetheless, quite effective. In the past it had not been possible to include the required components in small ordnance devices because of space limitations.

The evaluation, for ordnance use, of microelectronic fabrication techniques currently used in industry has begun. A circuit for the correlation detector comprising a Schmitt trigger and AND gate was supplied to industry in a request for quotation. Contracts were let to three companies for fabricating samples of thin film circuits with wired-in transistors, each using a different process, and a contract was also let for fabricating samples of an integrated-circuit version in which all components are formed by diffusion on a silicon substrate. These circuits will be given tolerance, performance and environmental tests to compare and to evaluate the different fabrication techniques.

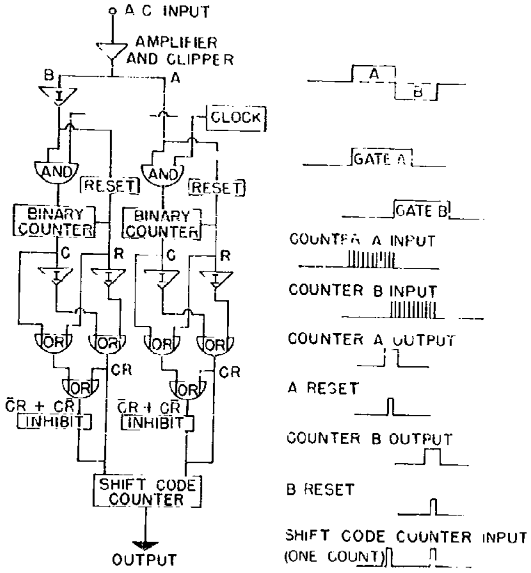
An additional project which is of interest here but is not a part of the program described above is the development of an rf-insensitive pnpn switch in an integrated configuration. The performance of the switch has been investigated in an equivalent lumped-circuit configuration and a contract has been let to fabricate samples in an integrated configuration.

Correlation Detector - A time gated system and a balanced mixer system are the two types of cross correlation detection being studied for detecting a signal of known frequency under low signal to noise conditions. Figure 1 is a diagram of the time gated system. The input signal is used to gate a clock into a binary counter which automatically resets when there is no input signal. With a fixed clock frequency the binary counter has a required gate time for the clock to count through and give an output. If the input signal is too high in frequency, the gate time will be too short and the counter will reset before there is an output. Coincidence between the counter output signal, which has a fixed time duration, and the reset signal is required to allow an input signal to the shift code counter. When the signal is too low in frequency coincidence between the reset and counter output does not occur and an input to the shift code counter is prevented. Figure 2 shows the band pass characteristics of the system and figure 3 shows the change in output counts for fixed signal level and frequency and increasing noise levels.

Figure 4 is a diagram of the balanced mixer system. The input signal, including its associated noise, is passed through a band pass filter which is of relatively wide band width, but reduces noise signals that could over drive the phase splitter. Signals from the phase splitter are then mixed with an internally generated reference signal of the same frequency and a lower side band frequency is obtained which is passed by the low pass filter to the difference amplifier. Output from the difference amplifier is used to control the forward and reverse shift gates of a shift register. Activation of the forward shift gate is necessary for a required length of time before an output from the shift register is obtained. The system was designed to operate on a signal level of 3 Vrms and figure 5 shows the band pass characteristics for 2, 3 and 4 Vrms signal levels. Figure 6 shows the band pass characteristics for 3 Vrms and no noise and 3 Vrms signal and 8 Vrms noise.

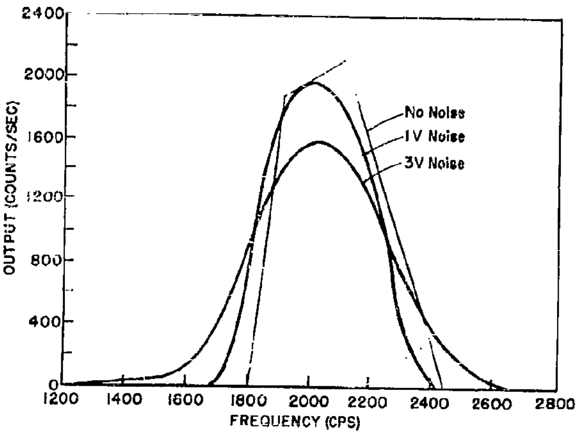
As described above, two types of cross correlation detector systems are being studied, and a typical sample circuit from one system is being fabricated in thin film form and in integrated circuit form. This circuit is shown in figure 7. Contracts have been let with three manufacturers, using different thin film processes, to fabricate samples of this circuit, and a contract has been let with one manufacturer for fabrication of this circuit in integrated form. Figure 8 is a chart showing the three companies Texas Instruments, Alpha Micro-electronics, and Intellux Inc. and their related thin film processes.

In the Texas Instrument thin film circuit approach resistors are made by sputtering a tantalum film onto a substrate, etching to form a resistor path, and then anodically oxidizing part of the film. The anodization process converts the outer portion of the film to a thin


A C INPUT
AMPLIFIER AND CLIPPER
B
A
CLOCK
AND
AND
RESET
RESET
BINARY COUNTER
BINARY COUNTER
C
R
C
R
OR
OR
OR
OR
CR
CR
OR
OR
C̄R + CR
INHIBIT
C̄R + CR
INHIBIT
SHIFT CODE COUNTER
OUTPUT
A
B
GATE A
GATE B
COUNTER A INPUT
COUNTER B INPUT
COUNTER A OUTPUT
A RESET
COUNTER B OUTPUT
B RESET
SHIFT CODE COUNTER INPUT
(ONE COUNT)

TIME-GATED SYSTEM

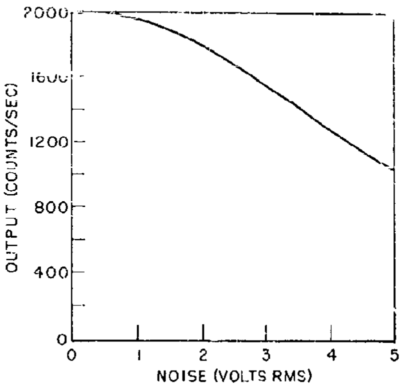
Figure 1



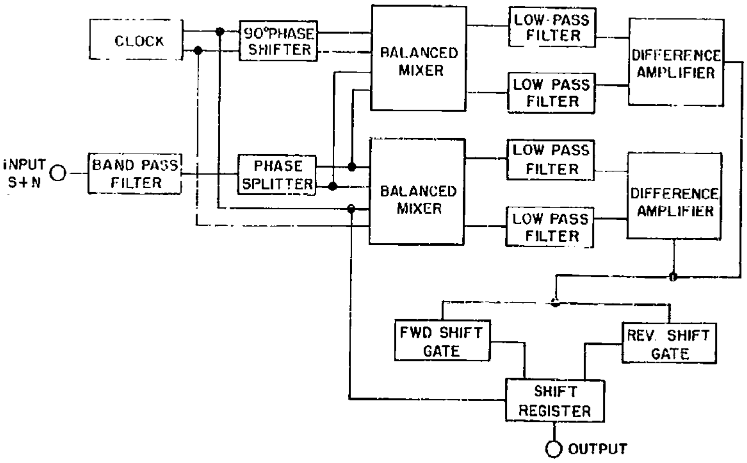
TIME-GATED SYSTEM
BAND-PASS CHANGE with NOISE LEVEL
(3V RMS SIGNAL)

Figure 2

Figure 3

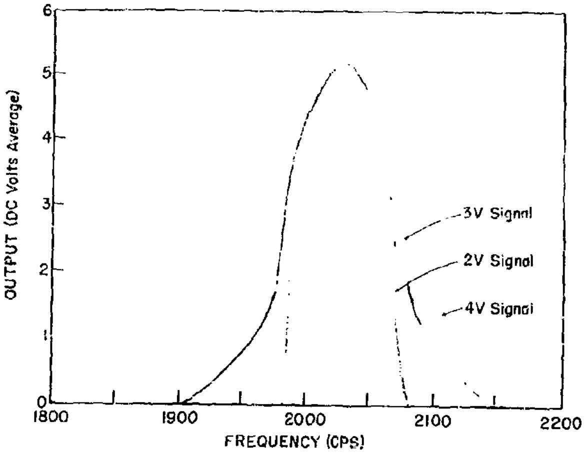


TIME-GATED SYSTEM
OUTPUT FALL-OFF with NOISE
(3V RMS SIGNAL)


CLOCK
90°PHASE SHIFTER
BALANCED MIXER
LOW-PASS FILTER
LOW PASS FILTER
DIFFERENCE AMPLIFIER
INPUT S+N
BAND PASS FILTER
PHASE SPLITTER
BALANCED MIXER
LOW PASS FILTER
LOW PASS FILTER
DIFFERENCE AMPLIFIER
FWD SHIFT GATE
REV. SHIFT GATE
SHIFT REGISTER
OUTPUT

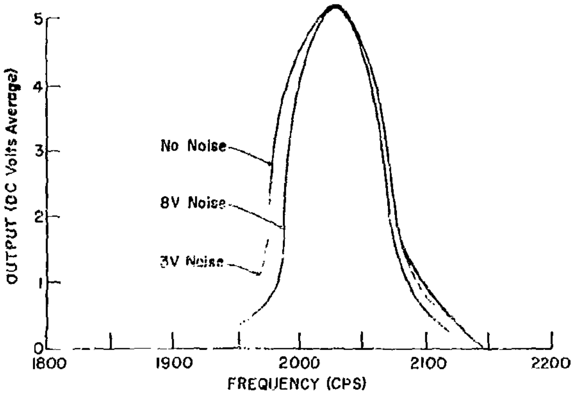
BALANCE-MIXER SYSTEM

Figure 4



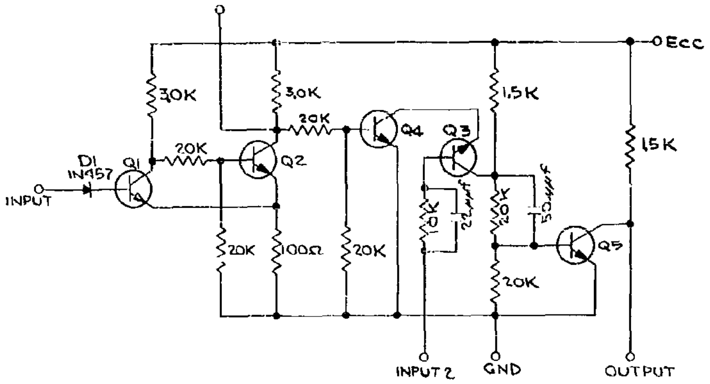
BALANCED-MIXER SYSTEM
BAND-PASS CHANGE with SIGNAL LEVEL
(No Noise)

Figure 5



BALANCED-MIXER SYSTEM
BAND-PASS CHANGE with NOISE LEVEL
(3V RMS SIGNAL)

Figure 6



Ecc
30K
3,0K
20K
20K
1,5K
15K
D1
1N457
Q1
Q2
Q4
Q3
Q5
INPUT
10K
22μμf
20K
50μμf
20K
100Ω
20K
20K
INPUT 2
GND
OUTPUT

NOTE:
Q NUMBERS ARE 2N914(FSP165 - MOLYTAB EQUIV)

AND GATE AND SCHMITT
TRIGGER CIRCUIT

U.S. NAVAL ORDNANCE LABORATORY

Figure 7

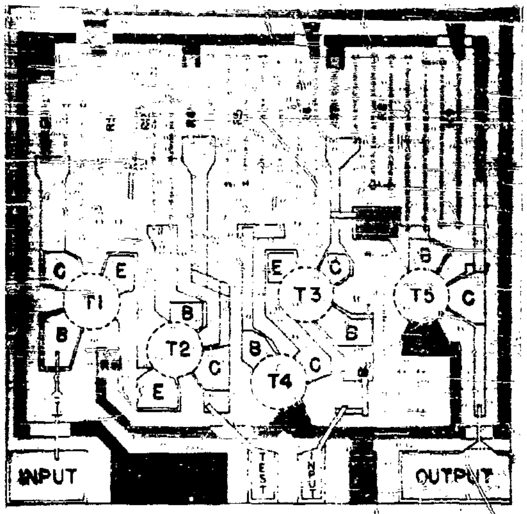
	AME	INTELLUX	TEXAS INSTRUMENTS
THIN FILM METHOD	VACUUM DEPOSITED	SPRAYED ON HOT SUBSTRATE AT ATMOSPHERIC PRESSURE AND PHOTO ETCHED	SPUTTERING, PHOTO-ETCHED
SUBSTRATE	GLASS OR CERAMIC	GLASS	CERAMIC
RESISTORS	NICHROME TOLERANCE 10% & 2%	TIN OXIDE - TOLERANCE 10% AND 1% ARE STANDARD TEMPERATURE COEFFICIENT 50 PPM/°C	TANTALUM 100Ω /SQUARE TEMP. COEFF. ±150 PPM/°C RANGE - 50-500 KΩ
CAPACITORS	PLATES-ALUMINUM DIELECTRIC-SILICON MONOXIDE	PLATES - TIN OXIDE OR COPPER DIELECTRIC - EPOXY OR BARIUM TITANATE	PLATES - TANTALUM V MAX = 50 V DIELECTRIC - TANTALUM OXIDE TEMP COEFF + 250 PPM/°C
CONDUCTORS	ALUMINUM	COPPER OR GOLD	TANTALUM
PROTECTION	SILICON MONOXIDE	GLASS FRIT	EPOXY SILICON GEL
INTERCONNECTION	SOLDER OR CONDUCTIVE EPOXY	SOLDER	HIGH TEMPERATURE SOLDER GOLD-PLATED NICKEL WIRE

Figure 8

adherent film of oxide which serves both as a means of precisely adjusting resistance value and as a protective coating for the finished resistor. The sputtered tantalum resistors have temperature coefficients of ± 150 ppm/°C (parts per million per °C) and nominal resistivities of 100 ohms per square. Tantalum film capacitors are formed in the same manner as resistors with the anodic oxide film serving as the capacitor dielectric and the base tantalum layer serving as one electrode. A conductive counter electrode film is evaporated on, in order to complete the capacitor and also to further increase the lead conductivity.

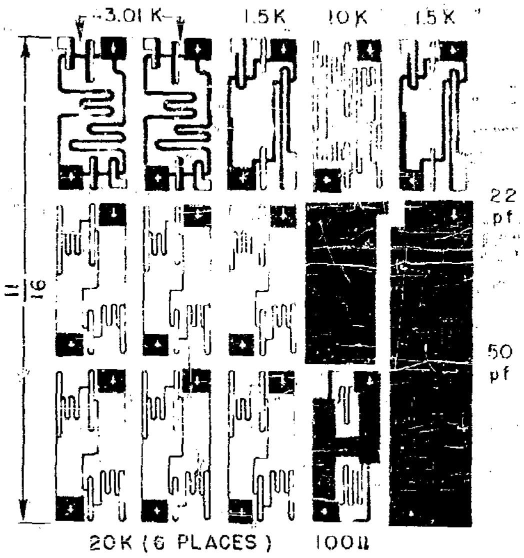
Figure 9 shows the sample circuit thin film layout of the thin film passive elements by Alpha Microelectronics. Resistors are made by resistance heating vapor deposition of nichrome in a vacuum. The vapor passes through a resistor pattern mask of bimetallic and is deposited in a thin film on a nickel and copper heated substrate to form a resistor path. The temperature of the substrate is adjusted to a value which insures complete film crystallization and adhesion of the metal to the substrate. Standard resistor tolerances are ±5% without trimming and have temperature coefficients of ± 200 ppm/°C (parts per million per °C). Nominal resistivity is 200 ohms per square. Capacitors are formed by vapor deposition of silicon monoxide film for the capacitor dielectric. The capacitor electrodes, and conductors for circuit interconnections are formed by vapor deposition of aluminum. A complete circuit is fabricated during one pump down of the vacuum chamber.

Figure 10 shows the sample circuit thin film layout of the thin film passive elements by Intellux. Resistors are made by spraying the surface of a heated glass substrate with a solution of a tin compound and catalytic agent. The materials in solution decompose when exposed to the high temperature substrate and a chemi-molecular bond with the substrate surface and a thin film of tin oxide is formed. The substrate, coated with a thin film of tin oxide, is etched by a photochemical process to form a resistor path. Small trimmer resistors are usually added in series with the required circuit resistors for adjustment to the desired tolerance. The tin oxide resistors have temperature coefficients


C
E
T1
B
B
T2
C
E
E
C
T3
B
B
C
T4
B
T5
C
INPUT
TEST
INPUT
OUTPUT

NICHROME RESISTOR PATTERN
FOR ST CIRCUIT

Figure 9


3.01 K
1.5 K
10 K
1.5 K
22 pf
50 pf
11
16
20K (6 PLACES)
100Ω

TIN OXIDE RESISTOR
PATTERN FOR
ST CIRCUIT

Figure 10

of ± 50 ppm/°C (parts per million per °C) and nominal resistivities of 10° ohms per square.

Capacitors are formed by depositing an epoxy resin film dielectric on a tin oxide base which serves as one electrode. A layer of copper is deposited over a protective coating of glass frit in which openings were left for feed through connections. The copper is etched by photochemical processes to form conductors for interconnections and a counter electrode for the capacitors.

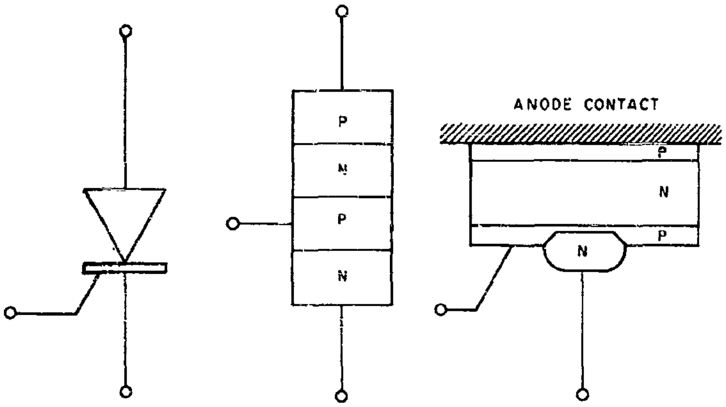
Texas Instruments has an integrated circuit form of the sample circuit. Resistors, capacitors, transistors, and diodes are fabricated within a single silicon wafer. The initial silicon slice has a very high resistivity and forms electrical isolation between the diffused areas. The dimensions and positioning of the diffused areas are accurately determined by photolithographic processing of a silicon dioxide coating formed on the wafer. Silicon dioxide is an effective masking agent for the diffusants used, and thus, diffused paths will be formed only where the silicon dioxide has been removed. During diffusion, silicon dioxide is re-formed over the entire wafer, protecting all electrical paths and surface area. After diffusion, deposited leads of aluminum are formed over the insulating surface of silicon dioxide providing point to point connection of the desired component areas into a particular electronic circuit. Assembly is completed by thermocompression ball bonding 1- mil gold from the surface of the network to the leads inside a header which is then capped and forms a hermetic seal. The sample circuit was fabricated from a standard basic wafer design of Texas Instrument which contains seven transistors, seven diodes, eight capacitors and nine resistors for possible use.

RF Insensitive Switch Development - The RF insensitive switch utilizes a silicon controlled rectifier which consists of four layers of p- and n-type silicon forming three interacting p-n junctions. From bottom to top in figure 11, these are, the emitter or cathode junction, the collector junction, and the conjugate emitter or anode junction. The lower two junctions form, in effect, a high gain n-p-n transistor, and the upper two junctions form a low gain p-n-p "transistor," both "transistors" having a common collector. The α of each "transistor" increases with collector current at low currents. Since the "transistors" are connected for positive feedback, the device switches "on" when the collector current rises to such a value that the sum of the α's exceeds unity. A forward voltage of about 1/2 volt must be placed across the emitter junction to raise the collector current to this value, and so any signal which can raise the gate voltage to this level can fire the switch.

A controlled rectifier has some inherent protection against RF signals introduced at its gate lead. The capacitance of its emitter junction combines with the resistance around the gate contact to form a simple RC filter which attenuates the RF. The action of this filter decreases the sensitivity of the switch as the frequency of the gate signal is increased, as is shown in figure 12 for two pnpn switches. Figure 13 shows a simplified diagram of the test circuit used.

Controlled rectifiers can also be fired by spurious RF applied between anode and cathode. In this case, the RF voltage is divided between the reactance of the anode capacitance and the impedance of the external circuitry feeding the gate. Figure 14 shows the test setup used to determine anode RF sensitivity. Figure 15, the increase of sensitivity with frequency at the lower frequencies, followed by the leveling off at higher frequencies agrees qualitatively with this model. Additional work is needed to explain the new increase of sensitivity at the highest frequencies checked. The 2N684 could not be fired at the RF voltages available, up to 60 v at 1 mc and 6 v at 40 mc.

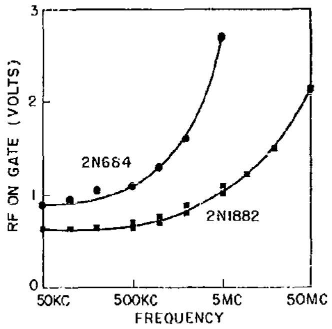
The voltage divider model of the controlled rectifier suggests two methods of protecting against RF which inadvertently reaches the anode. One method is to reduce the impedance of the external gate circuit, preferably by means of a gate capacitor to protect against the high frequencies to which the switch is most vulnerable. Figure 16 shows the effectiveness of this method at one frequency. The internal gate capacitance can be found by extrapolating the data to the DC gate


P
N
P
N
ANODE CONTACT
P
N
P
N

PNPN SWITCH
(SILICON CONTROLLED RECTIFIER)

Figure 11

Figure 12



RF FIRING OF TWO CONTROLLED RECTIFIERS

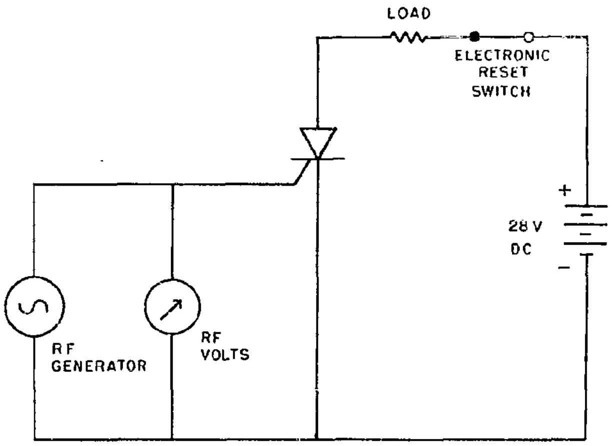
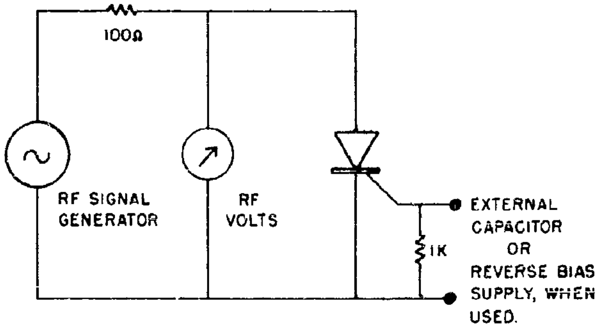

LOAD
ELECTRONIC RESET SWITCH
+
28 V DC
−
RF GENERATOR
RF VOLTS

Figure 13

SIMPLIFIED RF SENSITIVITY TEST

Figure 14


100Ω
RF SIGNAL GENERATOR
RF VOLTS
1K
EXTERNAL CAPACITOR OR REVERSE BIAS SUPPLY, WHEN USED.

SIMPLIFIED CIRCUIT TO TEST RESPONSE OF SCR TO RF ON ANODE

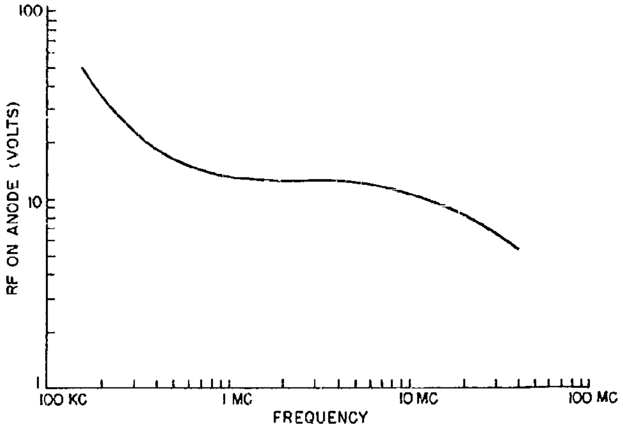
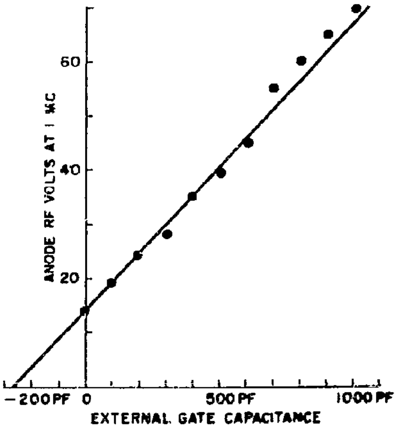


Figure 15

FIRING OF 2N1882 BY RF ON ANODE

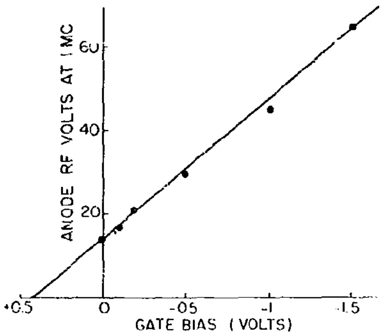
Figure 16



ANODE RF PROTECTION RESULTING FROM ADDITIONAL GATE CAPACITANCE firing voltage of about 1/2 volt. The other method is to apply a reverse bias to the gate. As figure 17 shows, the anode RF voltage for firing is increased in proportion to the reverse bias. The constant of proportionality is about 30 in this figure and can be improved greatly by means of the external gate capacitor mentioned before. The data extrapolate to the DC gate firing voltage of the switch. These methods permit considerable RF voltages to be placed on the anode without firing the switch, as long as the sum of RF and DC voltage does not exceed the maximum DC blocking voltage. However, while the switch will block DC in an RF environment, the RF is still coupled into the circuit by the anode capacitance.

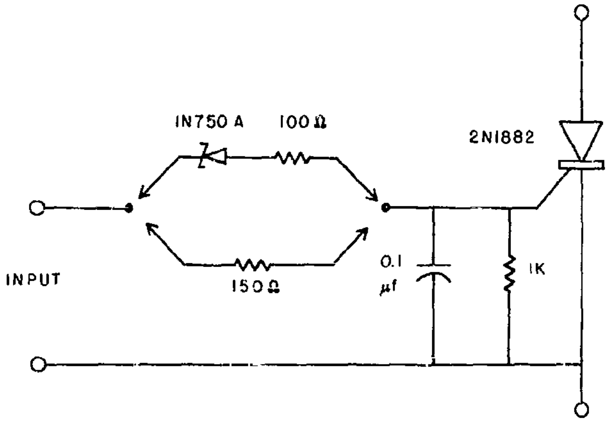
Placing a reverse bias on the gate should also increase the RF gate signal it can withstand, but only by the amount of the bias, which is limited by the emitter breakdown voltage. RF gate firing may also be prevented by removing the anode voltage during the times when spurious gate signals are likely to occur, but this is not always practical. Thus, it appears necessary either to prevent strong RF signals from reaching the gate, or to produce a switch which is less sensitive to them.

Much protection can be obtained by including an RC filter in the gate circuit, but an RC filter slows the response of the switch to pulses of DC. If fast switching is required, as well as insensitivity to RF, the upper variation of the circuit on figure 18 is preferable; since it can discriminate between fast DC pulses and RF signals. The series resistor and the capacitor form an RC filter to attenuate some of the RF. The zener diode serves to provide a greater voltage drop to positive half-cycle than to negative half-cycles, rectifying the RF signal and placing a desensitizing negative bias on the gate. The zener also provides a DC standoff voltage to prevent response to small spurious DC signals. The 1k resistor between gate and cathode is a bias resistor included for stability. The upper curve on figure 19 shows the results obtained with this circuit, while the lower curve shows the sensitivity for an ordinary RC protected switch with the same response time of .88 s to a 15 v DC input pulse. The



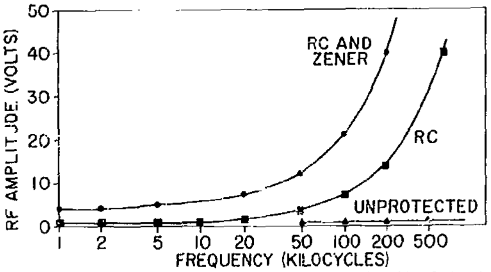
ANODE RF PROTECTION RESULTING FROM REVERSE GATE BIAS

Figure 17


1N750 A
100 Ω
2N1882
INPUT
150 Ω
0.1 µf
1K

TWO CIRCUITS TO PROTECT SCR GATE AGAINST RF

Figure 18



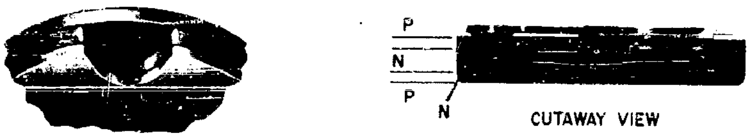
PERFORMANCE OF RF PROTECTION CIRCUITS

Figure 19

sensitivity of the unprotected 2N1882 is shown at the bottom for comparison.

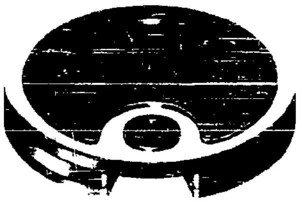
The zener circuit seems relatively easy to produce in integrated form by making a p-n zener junction at the gate contact instead of the usual ohmic contact. A contract has been let to International Rectifier to produce such a device. Figure 20 shows an early conception of the integrated switch. The small p-n junction to one side is the gate zener. The bottom two layers of silicon are shown etched away under the zener junction to prevent electrons injected on the negative half-cycles from diffusing to the collector and firing the switch. The oxide and gold layers should add to the gate capacitance after the cathode and gate have been optimized in other respects. Figure 21 shows the same switch assembled and ready for encapsulation.

It is hoped that eventually such modified controlled rectifiers may be used in RF environments without danger of unwanted activations. In the meantime, considerable protection can be provided for existing pnpn switches by means of gate capacitors, appropriate biasing, RF filters, and extensive shielding.



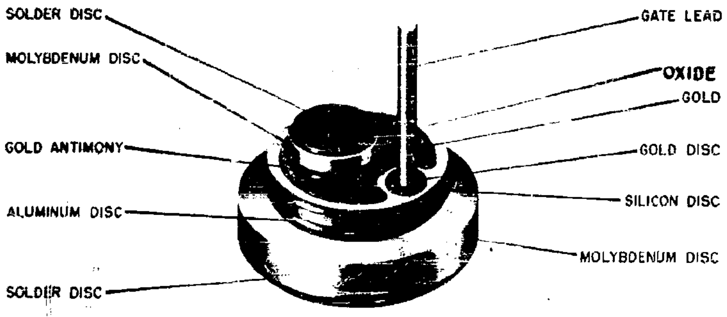
BOTTOM VIEW

CUTAWAY VIEW



TOP VIEW

Figure 20


SOLDER DISC
MOLYBDENUM DISC
GOLD ANTIMONY
ALUMINUM DISC
SOLDER DISC
GATE LEAD
OXIDE
GOLD
GOLD DISC
SILICON DISC
MOLYBDENUM DISC

JUNCTION ASSEMBLY

Figure 21

MICROWAVE SEMICONDUCTOR MICROELECTRONICS

Robert W. Yancey
U. S. Naval Ordnance Laboratory
Corona, California

I. INTRODUCTION

Microelectronics at its present state of development almost invariably presupposes the use of semiconductors for its active elements. Microwave microelectronics presents especially challenging problems since the researcher must extend the state-of-the-art in applying many semiconductor devices at these frequencies and simultaneously develop new circuit materials and substrates. However, the potential pay off is quite high if light, rugged, microwave systems can be shown to be applicable to aircraft and missile use. A study has been initiated at this Laboratory to develop and determine the properties of microwave functional circuits employing the advanced concepts of microelectronics and the best available semiconductor devices. Of particular emphasis during the initial period has been the application of the tunnel diode as an active microwave device.

II. SUBSTRATES AND CIRCUITRY

The properties of the substrate are of critical importance when it is attempted to use microelectronics at microwave frequencies. It is necessary to ascertain that the dielectric constant is uniform, that the substrate thickness is uniform and that one has the lowest possible dielectric losses. These requirements have been difficult to achieve with commercially available materials. In particular, uniform thickness has been a problem. There is one source now specializing in parallel plate, uniform dielectric, low loss, double clad laminate for microwave applications. More recently a machinable ceramic apparently with good microwave properties and a 5 micro-inch finish has become available. This material is to be studied at microwave frequencies. The latest development along this line is the announcement of a new method of depositing thin films on teflon and other fluorinated plastics with a good bond. After the substrate has been chosen the circuit must be formed by some suitable technique and thus more problems. Circuit thickness and smoothness are dictated to some degree by skin depth at the operating frequencies.

III. SEMICONDUCTORS

The present frequency limit of transistors is 2 Gc. Varactors provide very low noise amplifiers, but have a very limited bandwidth. Because of their higher frequency capabilities and broadband characteristics, tunnel diodes are used for local oscillators, detectors and amplifiers. At the beginning of this program the upper limit of commercially available diodes was 10 Gc. Now diodes are available capable of operating in the sixty to seventy (60 - 70) Gc range.

IV. RESULTS

To date L and X-band oscillators, an X-band autodyne converter and an L-band mixer-oscillator have been constructed using the microelectronics approach and tunnel diodes with very encouraging results. All of these circuits were constructed in and on double clad Rexolite using thick film and "pill" type components.

The L-Band oscillator is shown in Figure 1 below.

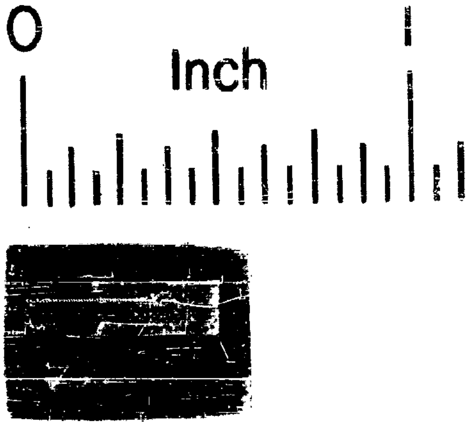


Figure 1 - L-Band Oscillator

The oscillator was constructed with a 20 Ma peak current diode and "microstrip" waveguide. The oscillator output was .5 milliwatts at 1.20 Gc. The frequency is sensitive to the supply voltage, thus a regulated supply must be used. The frequency may be varied up to approximately 1.22 Gc.

An L-band mixer-oscillator employing two (2) 3 Ma tunnel diodes was constructed. Using 10 Kmc tunnel diodes this circuit had the following characteristics:

Oscillator frequency	1.1 Gc	
IF frequency	30 Mc	
Noise figure	6.0 db	(approx.)
Conversion gain	2.0 db	
Bandwidth	.4 Mc	(determined by IF amplifier)
Min. detectable signal	-85 dbm	

This unit is shown in Figure 2 below.

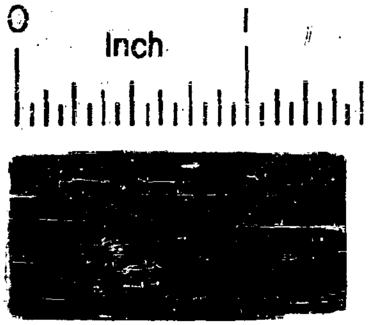


Figure 2 - L-Band Mixer-Oscillator

An X-band oscillator was constructed using a 3 Ma X-band diode. The construction was essentially identical to that of the L-band oscillator with the exception of the higher frequency diodes used. The output of this oscillator was approximately 5 microwatts at 9.44 Gc. This oscillator exhibited a voltage sensitive frequency variation as did the L-band oscillator.

The X-band converter tests are incomplete at this time so no performance figures are available yet.

Some of these devices were fabricated in order to increase our information concerning microelectronic microwave structures using semiconductors. The present effort is directed toward the development of low noise X-band (10 Gc) and Ka-band (35 Gc) microelectronic amplifiers. These will permit the fabrication of microwave receivers which require only a small fraction of the space, weight, and power required by present day equipment.

V. SUMMARY

Because of the complexity of semiconductor and microwave applications, each of which entails considerable specialization, there must be a great dependence upon sources outside the group for information. The employment of microelectronic techniques to the microwave portion of the electromagnetic spectrum has been essentially untouched. Progress has been delayed to a large degree by the additional requirements made mandatory by the behavior of microwaves.

One aspect not previously mentioned, but which is of prime importance, is cost. The cost of circuit preparation including masks and negatives may exceed the cost of some microwave structures. Several units would be far less expensive to produce in the microelectronic version than in the machined version with greater uniformity in addition to all of the other benefits of employing this approach.

POTENTIAL APPLICATIONS OF MICROELECTRONIC TECHNIQUES TO ASW WEAPON SYSTEMS

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University Park, Pennsylvania

The Ordnance Research Laboratory is not currently engaged in the microminiaturization field either as a doer or as a user. There are, however, several programs currently underway at the Laboratory that may require these techniques. I would, therefore, like to briefly discuss each of these programs to indicate the general nature of the electronics involved.

(1) Digital Data System

ORL is building a digital data-handling system to achieve practically automatic reduction of data from our test programs. An integral portion of this system is torpedo-borne data-collection unit. This unit is basically an analogue-to-digital converter with a multiplexer on the analogue input side capable of handling up to 45 analogue input signals. Conversion rate of the system is 6000 analogue samples per second. The digital data is recorded on magnetic tape at a density of 300 bits per track. This equipment is shown in Fig. 1.

(2) Torpedo Guidance System

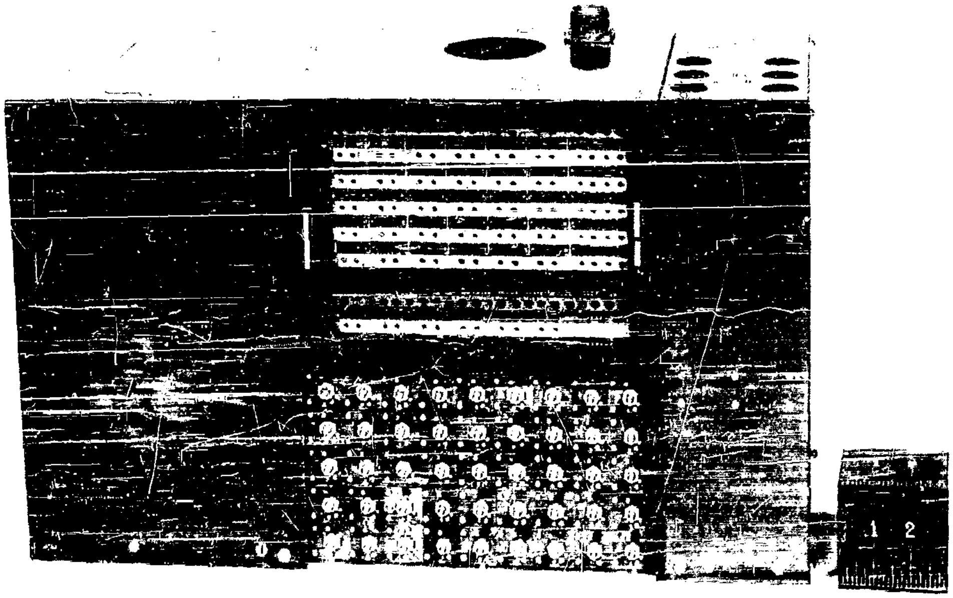
The feasibility of a multibeam signal-processing system employing correlation detectors is being investigated for torpedo application. A large number of parallel detection channels are required because of (1) the high doppler resolution and (2) the multibeam hydrophone. During the initial field tests of this system, a submarine will be used as a test vehicle.

Further development, to incorporate the signal-processing equipment in a torpedo, will probably require the use of microminiaturization techniques.

(3) Submarine-Borne ASW-Weapon Tracking System

A program was recently initiated at ORL to design and develop an ASW-weapon tracking system. The system will be installed in the target submarine. The system will require the installation of acoustic receiving and transmitting equipment in the ASW weapons. The space and weight limitations in the weapons may require microminiaturization of the weapon equipment to be installed.

A wide variety of both analogue and digital circuits is required to design these systems.



The Microelectronics Laboratory at Johns Hopkins University Applied Physics Laboratory

William Liben
Johns Hopkins University Applied Physics Laboratory
Silver Spring, Maryland

The Microelectronics Laboratory at the Applied Physics Laboratory was activated in November 1960. The decision to do so was made after a careful study of the potential applications of microelectronic methods of electronic system fabrication to weapons systems of interest to the Laboratory.

The proposed effort was to be divided into three areas of interest: (1) Research on components, devices, materials and procedures of interest in microelectronics; (2) Fabricate prototype systems for use in Laboratory systems; and (3) Work with vendors and Laboratory system designers in procuring microelectronic hardware.

Financial support was provided, from the beginning, by RMGA-8, Advanced Technology Section and RREN-4, Advanced Components Engineering, both of the Bureau of Naval Weapons.

All of the methods which have been proposed for the fabrication of microelectronic circuits are based upon two broad ideas: (1) The manipulation of semiconductors to produce electronic circuits. The operation of these circuits depends upon the three dimensional properties of the resulting devices. For this reason the semiconductor systems have been classified as "bulk circuits". (2) The use of thin films of dielectric and conductive materials to fabricate a complete electronic circuit, classified as a "thin film circuit".

We have decided to work in both the bulk and thin film circuit areas for the sake of completeness. At the present time all bulk circuit fabrication is based upon planar diffusion technology. The starting point is a wafer of Silicon which is .003 - .010" thick. Components and devices are made in this wafer by selective doping to produce n and p elements of desired dimensions and junctions.

The method we propose to implement can be illustrated by the steps required to fabricate a bulk resistor. (See Fig. 1) The value of a resistor is fixed by the resistivity, length, width and thickness. The length and width are delineated by a masking procedure. The surface of the Silicon slice is converted to Silicon dioxide by exposure to high temperature steam. A photoresist is applied to the oxide. All but the resistor area is exposed to ultra-violet light and developed. The exposed photo-resist is firmly fixed in place and thereafter acts as a stop-off resist during chemical etching action. The unexposed areas of photo-resist are removed from the oxide during developement. The Silicon wafer is now immersed in a fluoride etch which removes the exposed Silicon dioxide. This exposes the pure Silicon over a selected area where the resistor will be diffused. The remainder of the slice is protected by a layer of Silicon dioxide or quartz. Quartz is notorious for its stability at high temperatures. It therefore acts as a stop-off film during the high temperature diffusion operation performed next.

The unprotected area is now converted to n or p material to a desired depth by exposing the wafer to a predetermined concentration of doping atoms at a predetermined temperature for a predetermined time. This results in a filamentary resistor as shown in Fig. 2.

Successive applications of the above procedure results in the fabrication of resistors, p-n junctions which act as diodes, and transistors. Complete circuits may be as small as .050" X .050". Since commercial Silicon wafers are available in 1" diameters, a large number of identical circuits can be fabricated in a single procedure. This is one of the advantages of the bulk method.

In the case of the thin film circuit the choice of the fabrication method is not as clear cut. Present capability is limited to the fabrication of conductors, resistors, and capacitors, and inductors of limited value. Active devices and diodes cannot yet be fabricated by thin film procedures. Since most of the research work on active devices uses the vacuum evaporation fabrication method, and this method appears to be the most versatile in its ability to use the greatest variety of materials to fabricate thin films, it would appear that the vacuum evaporation method offers the greatest hope for developing a compatable circuit fabrication procedure. By this I mean a single procedure suitable for the fabrication of a complete circuit preferably in one operation. For this reason we have elected to work with the vacuum evaporation method in making thin film circuits.

The critical laboratory operations are in an area which is being converted to a clean room area. The conversion of this space to a "clean" area is nearly complete. (See Fig. 3) In the clean room area is located the following work areas: (1) Bulk diffusion furnace room. This room has six diffusion and two source furnaces, guaranteed stable to $\frac{1}{2}$°C, a vacuum evaporator for evaporating conductive paths on the Silicon wafers, and eventually an epitaxial crystal growth system. Due to the large power dissipation in this room, it is serviced by its own 7$\frac{1}{2}$ ton airconditioning unit and electrostatic dust precipitator. The remainder of the clean room area is serviced by a 10 ton airconditioner and electrostatic dust precipitator. (2) The vacuum evaporation laboratory presently contains three 18" and one 14" evaporator. One of the 18" evaporators is equipped with a four position mask changer and is used for fabricating thin film circuits. The other three are being used for research work. (3) An instrument room wherein is available precision measuring instruments. At present we have an Ainsworth Micro-balance for weighing thin films to an accuracy of one microgram, a Bausch and Lomb metallurgical microscope which doubles as a multiple beam interferometer, a Nikon optical projection comparator to make measurements precise to .0001" on masks, thin film and bulk circuits and a three point probe to make measurements of the values of bulk and thin film components. (4) A photographic processing room containing a dark room, an ultra-violet source for exposing photo-resist, and a Burke and James precision camera for photographically reducing circuit art work by factors of 10 or 20 onto high resolution glass plates. (5) A chemical room used for a variety of chemical procedures on the Silicon wafer, such as etching of quartz masks, stripping of resists, cleaning and protection of substrates. (6) Step and repeat camera room which contains our X-Y coordinategraph used to make large scale art work and where a step and repeat camera will be added for the preparation of the films used to expose the photo-resist on the Silicon wafers. (7) White Room used for testing of circuits and thermocompression and

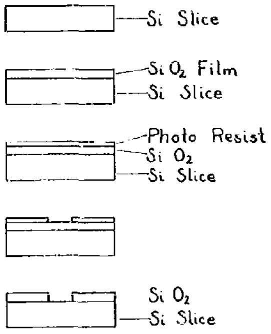

Si Slice
Si O$_2$ Film
Si Slice
Photo Resist
Si O$_2$
Si Slice
Si O$_2$
Si Slice

Fig. 1 - Semiconductor masking and photo resist procedures

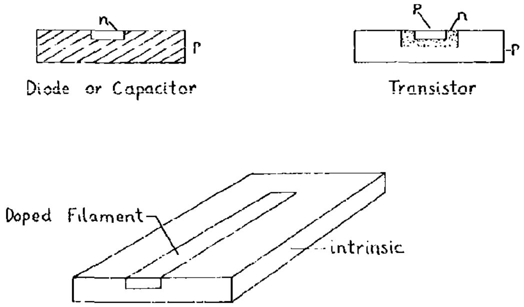

n
p
Diode or Capacitor
p
n
p
Transistor
Doped Filament
intrinsic

Fig. 2 - Bulk devices made by diffusion

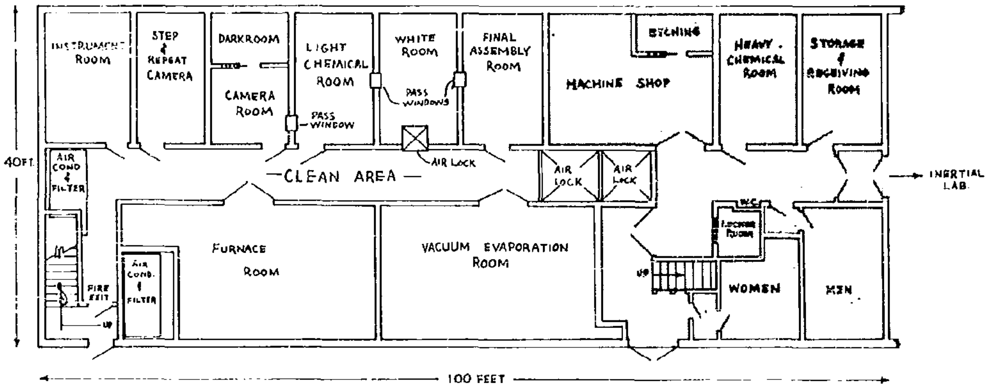

INSTRUMENT ROOM
STEP & REPEAT CAMERA
DARKROOM
CAMERA ROOM
LIGHT CHEMICAL ROOM
PASS WINDOW
WHITE ROOM
PASS WINDOWS
FINAL ASSEMBLY ROOM
ETCHING
MACHINE SHOP
HEAVY CHEMICAL ROOM
STORAGE & RECEIVING ROOM
AIR LOCK
AIR LOCK
AIR LOCK
CLEAN AREA
INERTIAL LAB.
40FT.
AIR COND & FILTER
FIRE EXIT
UP
AIR COND. & FILTER
FURNACE ROOM
VACUUM EVAPORATION ROOM
W.C.
LOCKER ROOM
UP
WOMEN
MEN
100 FEET

Fig. 3 - Microelectronics Laboratory space arrangement

ultrasonic bonding of wires on circuits. (8) Assembly and packaging room.

Outside the clean room area we have a machine shop, chemical spray etching, water still, vapor degreaer and a material storage area.

The second floor has one room with grinding and polishing equipment for the Silicon wafers, two electronics laboratories, and office space.

Functionally the group is organized into three projects. One is concerned with thin film microelectronics, another with semiconductor or bulk microelectronics, and the third with microelectronic circuit design. Microelectronic circuit design is substantially different from the design of conventional circuits due to the limitations imposed by the methods of fabrication.

During the past year a substantial portion of our time was concerned with setting up our facilities and we are still concerned with this problem. However, we have been able to work on some fabrication problems and do some research.

A problem which was selected as a vehicle for developing our thin film fabrication facility, was a 15 mcs receiver which was intended to be used as a brain stimulator in studying animal responses to electrical pulse stimuli. The specifications for the receiver were supplied by the Section on Neurophsychology at the National Institute of Mental Health. This system was selected as a test vehicle since its specifications will remain fixed for a period of time compatible with the time required to develope and explore the capabilities of the thin film technology. Thus the system, when completed, will not be obsolete. A circuit has been developed which can be fabricated by evaporation procedures except for the transistors and one capacitor.

The function of the Thin Film System is to permit remote stimulation of electrodes which have been implanted in a monkey's brain shortly after its birth. The receiver is a single channel receiver capable of delivering a pulse having variable repitition rate (10 - 200 pps), width (0.1 - 10 ms), and height (0.1 - 2 ma) into a load which may vary between 1 and 10 K ohms.

The transmitter emits an amplitude-modulated 15-mcs pulse having a controllable width and repetition rate. The frequency of the amplitude modulation can also be controlled over approximately a two-to-one range. The low frequency end of this range is also independently adjustable, thus, providing a means of compensating for variations in the manufacture of the thin film receiver. The receiver functions as follows: (See Fig. 4)

Transistors Q-14 and Q-15 provide video amplification of the 15-mc carrier. The modulation is detected, amplified, and limited by Q-16 and Q-17. The output of Q-17 is a square wave driving the distributed RC filter. The interaction of this square wave with the filter serves to provide the means of varying the height of the receiver output pulse. The design is such that the modulation frequency always falls on the skirt of the filter's characteristic. Thus, as modulation frequency is varied (at the transmitter), the filter input signal remains constant because of the limiting; however, the filter output signal varies in amplitude. This signal is then processed in the third substrate to yield a dc signal proportional to the modulation frequency. Since the width and repetition rate of the pulse is controlled at the transmitter, the other characteristics of the output are obtained.

Two samples of the receiver have been completed and work as expected. (See Figures 5, 6 and 7) We are now developing an antenna which can be packaged with the receiver in the allowed space.

A semiconductor frequency divider for use in the Transit Satellite is under development. This frequency divider is used to provide stable frequency steps required to control the satellite information processing. It was decided to start by constructing a divider from commercially available semiconductor circuits. The Texas Instrument "Solid Circuits" were selected because of their low power consumption. Due to the limitations of present fabrication techniques, the high frequency end is to be made of conventional components and will be miniaturized later as our capabilities develope.

The problem of breadboarding systems using the packaged semiconductor circuits can be difficult. Ordinary soldering procedures can easily injure the circuit package and they are expensive. A test module was deleloped and is shown in Fig. 8. An etched circuit board is prepared with a set of depressions into which the circuit package fits. Ten etched wires radiate from the depression and terminate in banana jacks. A Lucite clamp straddles the package clamping the flat leads to the etched wires. Fig. 9 shows twelve packages clamped in

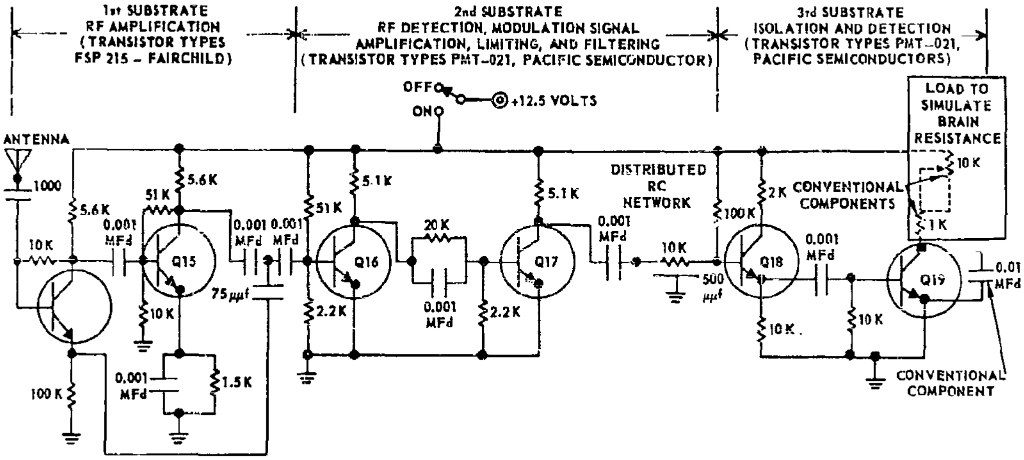

1st SUBSTRATE
RF AMPLIFICATION
(TRANSISTOR TYPES
FSP 215 - FAIRCHILD)
2nd SUBSTRATE
RF DETECTION, MODULATION SIGNAL
AMPLIFICATION, LIMITING, AND FILTERING
(TRANSISTOR TYPES PMT-021, PACIFIC SEMICONDUCTOR)
3rd SUBSTRATE
ISOLATION AND DETECTION
(TRANSISTOR TYPES PMT-021,
PACIFIC SEMICONDUCTORS)
OFF
ON
+12.5 VOLTS
LOAD TO
SIMULATE
BRAIN
RESISTANCE
ANTENNA
1000
5.6K
51K
5.6K
0.001
MFd
10K
Q15
10K
100K
0.001
MFd
1.5K
0.001
MFd
0.001
MFd
75μμf
51K
5.1K
Q16
2.2K
20K
0.001
MFd
2.2K
5.1K
Q17
DISTRIBUTED
RC
NETWORK
0.001
MFd
10K
500
μμf
100K
2K
CONVENTIONAL
COMPONENTS
10K
1K
Q18
0.001
MFd
10K
10K
Q19
0.01
MFd
CONVENTIONAL
COMPONENT

Figure 4 - Fifteen mcs FM Receiver

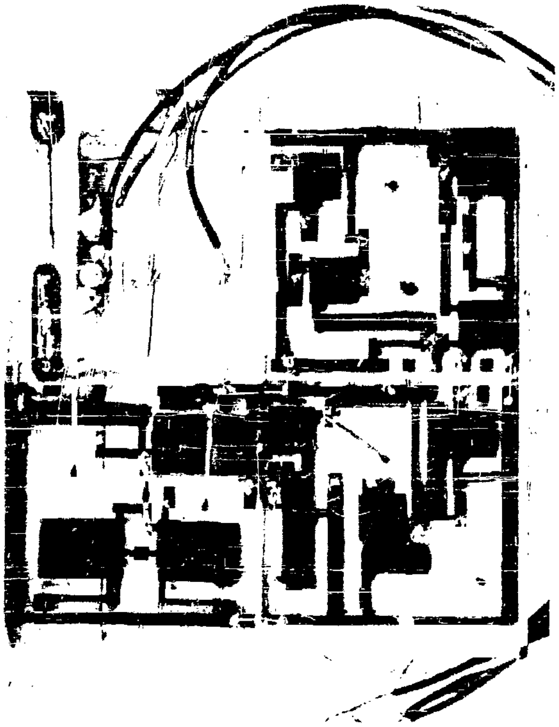


Figure 5 - Thin Film 15 mcs Receiver

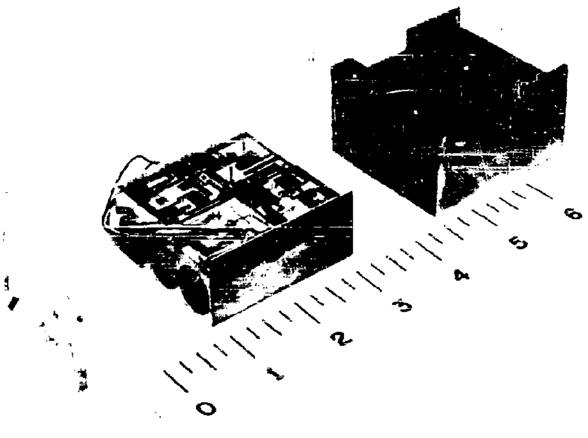


Fig. 6 - Exploded view, 15 mcs receiver assembly

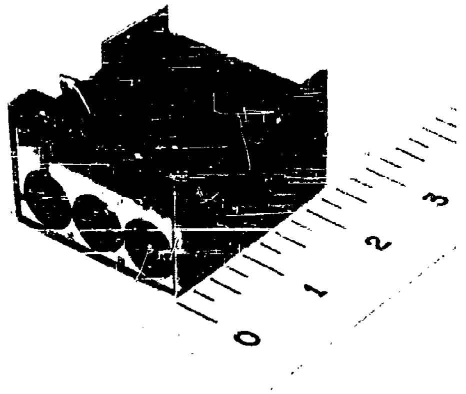


Fig. 7 - Complete 15 mcs Receiver Package

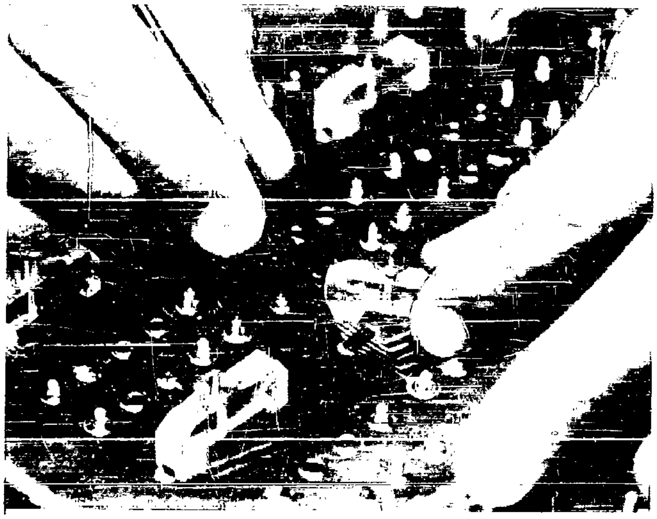


Fig. 8 - Test Module clamp for bulk circuit

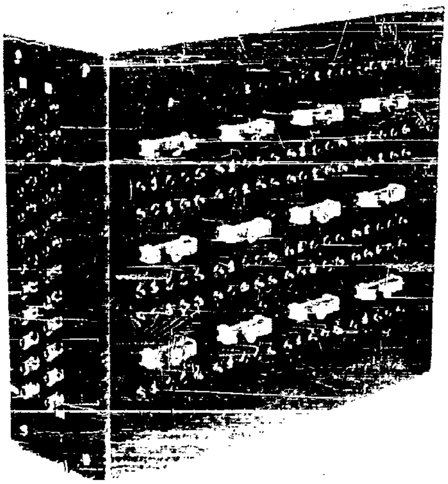


Figure 9 - Test Module for flat package bulk circuits

place. The packages are interconnected by patch cords on the reverse side of the etched board.

A method of assembling the Solid Circuit package has been developed which meets the following requirements:

1. The maximum possible packaging density consistent with reasonable unit volume power dissipation.

2. To follow Navy recommendations for microelectronic packaging as set forth in the Proposed Guide for Microelectronic Standards.

3. A relative ease of fabrication consistent with mechanical strength.

4. Ease of interconnection determination, layout, and realization.

5. No bending or twisting of semiconductor element leads and a minimum stress and strain on element leads during and after packaging.

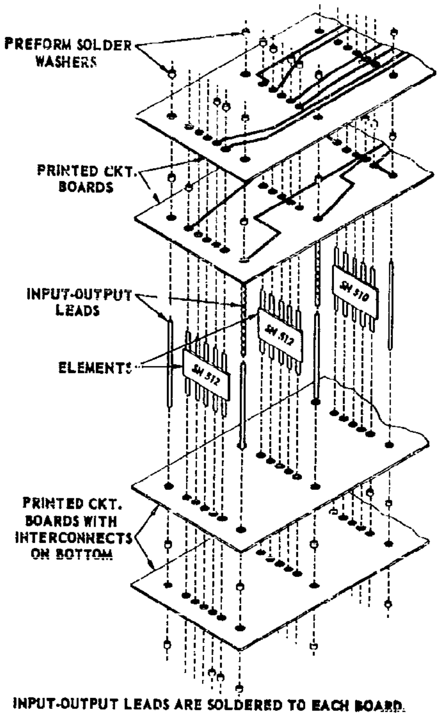
An exploded view of the first three elements of the proposed module is shown in Fig. 10. The overall dimensions of a finished module are:

Length - 0.6-inch
Width - 0.4-inch
Height - 0.2 - to 0.3 inch

The height of the module is determined by the number of printed circuit boards necessary for interconnection realization.

An optical soldering technique has been developed which consists of a high intensity light source focussed to a spot. Using projection lamps, high temperatures have been obtained (600° - 800^oF) but also large spot sizes. Small spot sizes are desired so only the solder washer and the conductors are heated, as heating the printed circuit board affects the bond between the copper and the board. At present a carbon arc is being used. A carbon arc reduces the spot size as the arc source is smaller than the lamp source, and the carbon arc does not have the controllability inherent in the projection lamp, but this does not appear to be as detrimental as a large spot size.

Fig. 11 is an exploded view of the circuit


PREFORM SOLDER WASHERS
PRINTED CKT. BOARDS
INPUT-OUTPUT LEADS
ELEMENTS
SH 510
SH 512
SH 512
PRINTED CKT. BOARDS WITH INTERCONNECTS ON BOTTOM

INPUT-OUTPUT LEADS ARE SOLDERED TO EACH BOARD.

ELEMENT LEADS ARE ONLY SOLDERED TO BOARDS WHERE INTERCONNECTIONS ARE TO BE MADE.

Fig. 10 - Exploded view of three elements of a bulk system module

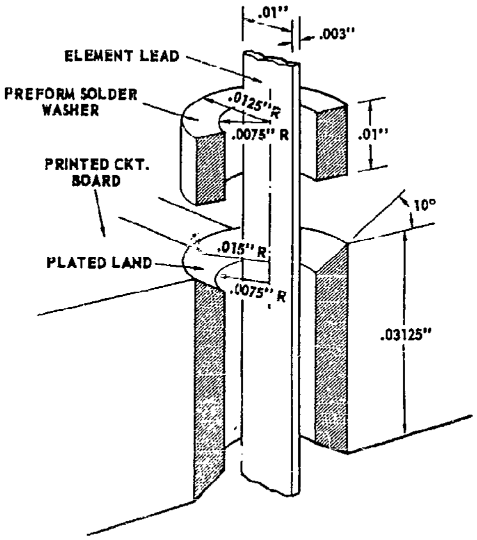

.01"
.003"
ELEMENT LEAD
PREFORM SOLDER WASHER
.0125" R
.0075" R
.01"
PRINTED CKT. BOARD
10°
.015" R
PLATED LAND
.0075" R
.03125"

Fig. 11 - Detail of Light Beam Soldering Preassembly

board, the flat lead wire and the solder preform before soldering. Fig. 12 shows the circuit package leads soldered to an etched circuit board. The leads are on .047" centers.

A serious limitation of present thin film resistor fabrication methods is the limitation of maximum values to about 250 K ohms within the available space. The solution to this problem is undoubtedly in the direction of producing film of large values of ohms/square. One approach is to fabricate films which are mixtures of insulators and conductors. This is the approach being followed by IBM in their work on the cermet resistor which is a mixture of silicon monoxide and chromium. The fabrication of these cermets is usually a more difficult procedure than the fabrication of pure metal resistors. So we are attempting to make large value resistors using the refractory metals tungsten and rhenium.

The vaporization temperatures of the refractory metals is so high (about 3000°C) that they are usually evaporated from a rod of the pure metal heated by electron bombardment. Therefore a vapor source was constructed (See Fig. 13) wherein electrons from a tungsten wire loop were accelerated by 5000 volts to the end of a metal rod 1/8" in diameter. The current magnitude is controlled by varying the temperature of the electron emitter. The electrons were focussed onto the tip of the rod by the two focussing plates. With this vapor source it was possible to produce resistors of 400 ohms/square in approximately 100 seconds when placed 8 inches from the substrate.

Initial experiments were with tungsten and almost immediately one fact became evident. The use of SiO as a protective overcoat was a bad choice. Adding the SiO changed the resistance as shown in Fig. 14. The shape of this curve can be explained if we assume that a surface layer of the tungsten film is converted to an oxide by the residual oxygen in the vacuum chamber before the SiO is added. When the SiO is added it converts to quartz by removing oxygen from the oxide freeing tungsten and so decreasing the resistance. Furthermore this effect should decrease in magnitude as thicker films are used, as it does in practice.

For this reason it was decided to try magnesium fluoride as an overcoat and indeed no change in resistance was found. The temperature coefficient of resistance is shown in Fig. 15, and the aging characteristic in Fig. 16. Apparently W films protected with MgF_2 are

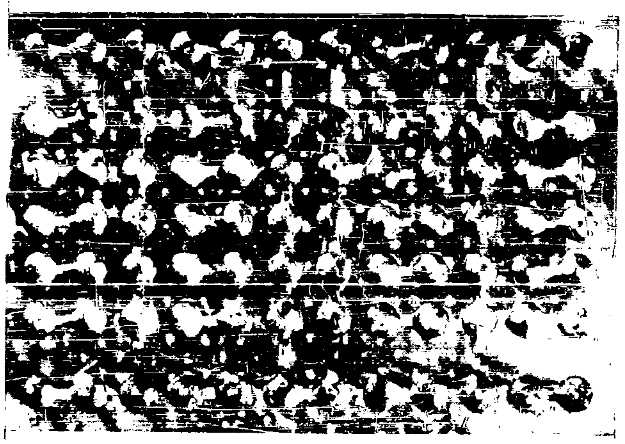


Figure 12 - Matrix of Soldered connection done with light beam

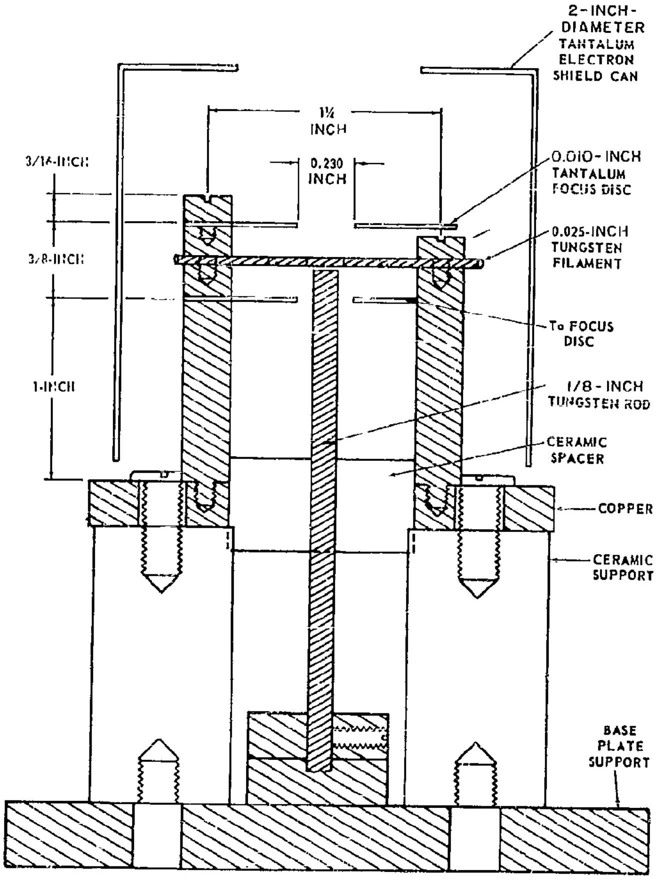

2-INCH-DIAMETER TANTALUM ELECTRON SHIELD CAN
1¼ INCH
0.230 INCH
3/16-INCH
3/8-INCH
1-INCH
0.010-INCH TANTALUM FOCUS DISC
0.025-INCH TUNGSTEN FILAMENT
To FOCUS DISC
1/8-INCH TUNGSTEN ROD
CERAMIC SPACER
COPPER
CERAMIC SUPPORT
BASE PLATE SUPPORT

Fig. 13 - Cross-section of electron bombardment vapor source

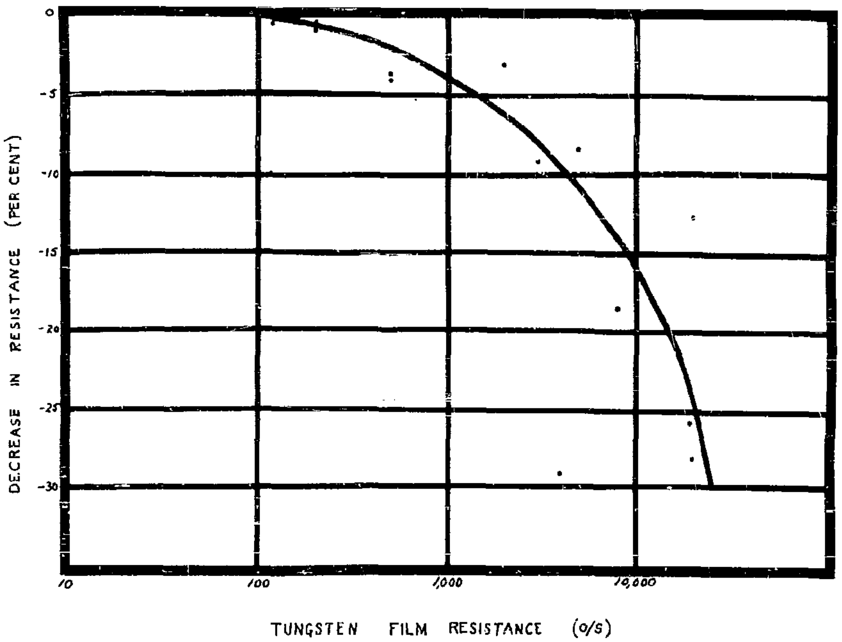


Fig. 14 - Decrease in Resistance of Tungsten Film When Protective Coat of SiO Initially condenses on Film Surface

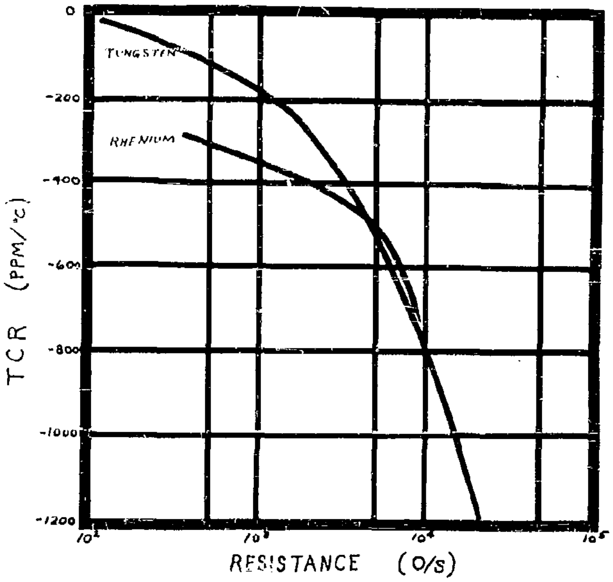


Fig. 15 - Temperature Coefficient of Resistance of Tungsten and Rhenium

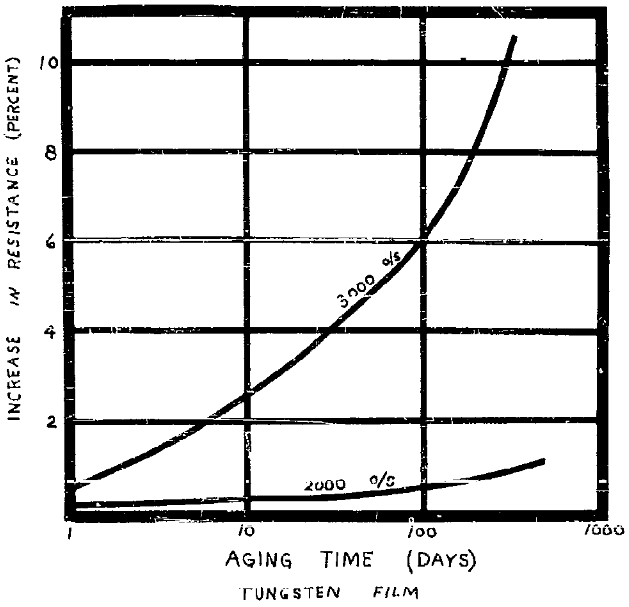


Fig. 16 - Aging of Tungsten films (no load)

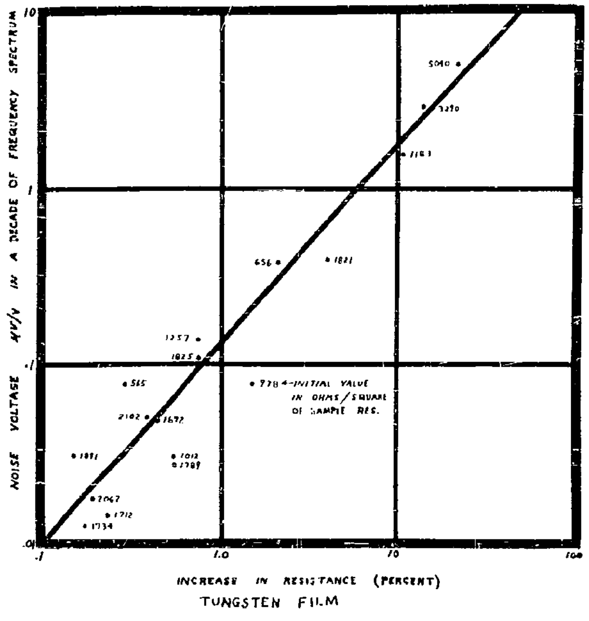


Fig. 17 - Current Noise Tungsten
Film Resistors

useful to about 2000 ohms/square. Aging was at room temperature with no applied load.

Noise measurements were made using a standard test developed at the National Bureau of Standards. In this test a fixed D.C. current is passed thru the resistor and the noise voltage in a frequency decade is measured and referred to 1µv/volt of D.C. on the resistor. On the whole the noise values for the tungsten resistors were somewhat less than those measured for $\frac{1}{4}$ watt composition resistors. It is apparent that there is a strong correlation between the current noise and the aging characteristic and not much with thickness. (See Fig. 17)

The same evaporation technique was used to make rhenium resistors which also were overcoated with magnesium fluoride. This apparently was a mistake since on aging, the films appeared to disappear from the slide. Presumably this was a result of reacting with the fluoride overcoat. It reinforces our belief that the nature of the protective overcoat is very important. Films from 3000 to 8500 ohms/square disappeared in one month, 2000 ohms/square in two months, 500 and 1000 ohms/square in three months.

Crane at Stanford University has described a signal propagating device which handles electrical signals in a manner similar to the way the human nervous system handles signals, and named it the neuristor. Furthermore, he has shown that if such a device were available it could be used to make all digital logic functions, and probably be useful in fabricating intelligent machines. No one as yet has been able to construct a neuristor in useful form. A useful neuristor should be small, cheap and producible in large numbers. Microelectronics fabrication methods should be useful here.

A semiconductor device has been postulated by Cote at APL which might behave as a neuristor. The idea is an extension of the tunnel diode principle, expanding a tunnel diode from a circular dot to a linear pn junction with the properties of tunnel junction material. (See Fig. 18) If a pulse is injected at one end to breakdown the junction it is hoped that this pulse will propagate down the linear junction. Such a device would be producible by semiconductor microelectronic methods.

As a start on our hardware procurement program we are in the process of selecting a contractor to fabricate three samples of a system used in the Typhon missile. In our first contract we decided to use thin film techniques, and selected a system wherein nearly all the passive components are capable of being evaporated, and both analog and digital circuitry are used.

Invitations to bid were sent to twenty-five contractors, and thirteen submitted proposals. Six of the proposals were judged to be good enough to merit further investigation. Visits were made to the six to select those with production facilities.

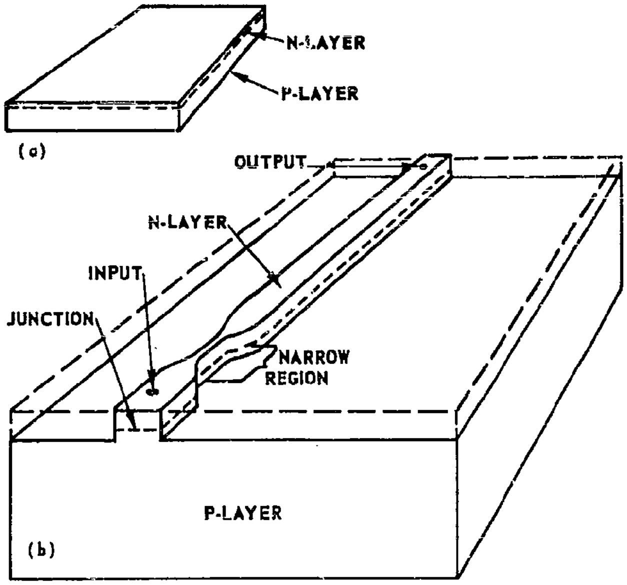

N-LAYER
P-LAYER
(a)
OUTPUT
N-LAYER
INPUT
JUNCTION
NARROW REGION
P-LAYER
(b)

Fig. 18 - Semiconductor Neuristor

NRL CONTRIBUTIONS TO THE MICROELECTRONICS PROGRAM

C. V. Parker
U. S. Naval Research Laboratory
Washington 25, D. C.

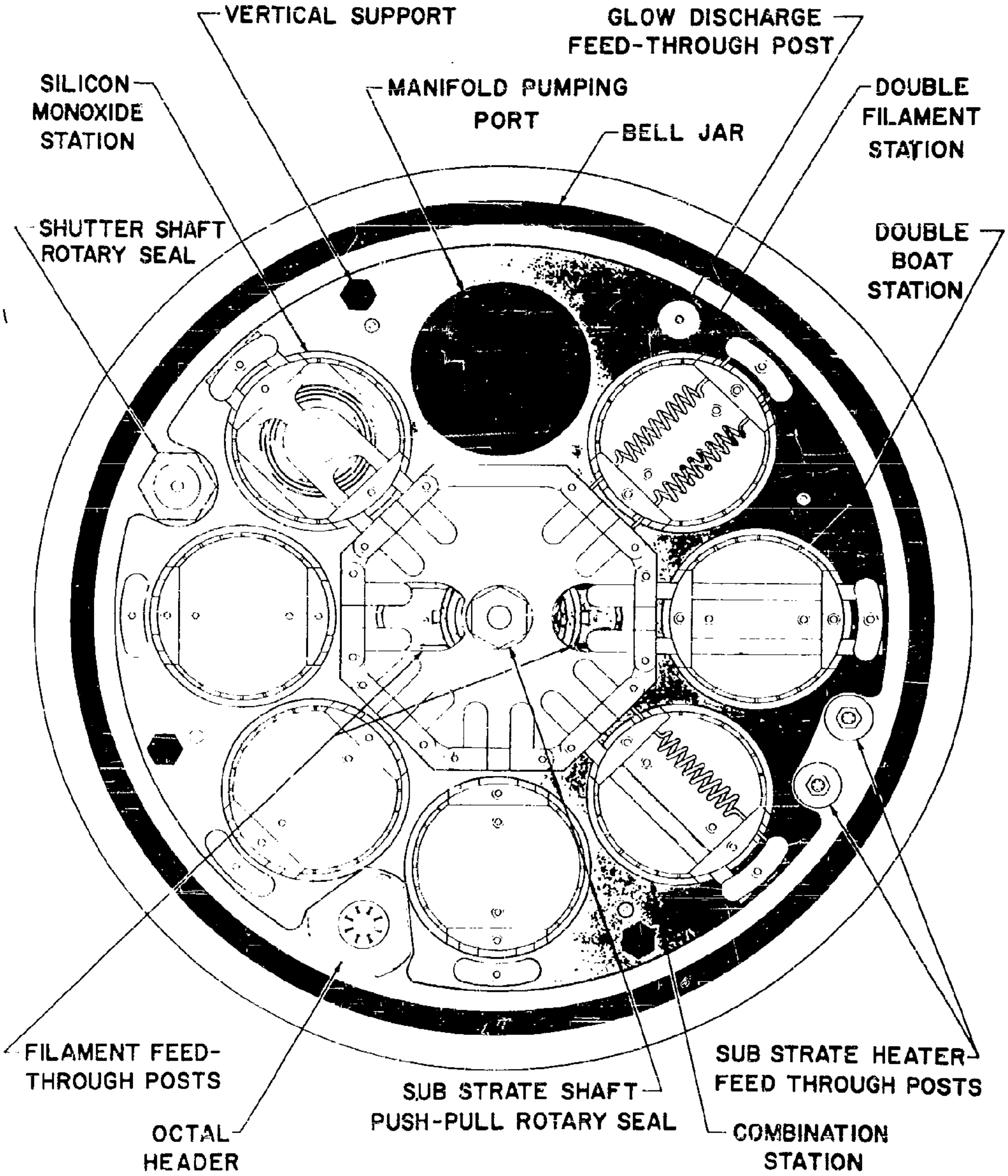
It was pointed out at the Navy Laboratory Microelectronics Program Conference held last year that much of the research work being done at NRL, particularly in the materials area, has a potential bearing on microelectronics and constitutes basic research support for it. In general, this work is continuing and is regularly reported in the "Report of NRL Progress", a monthly journal.

My discussion will be limited to certain areas of work which may be of most interest to the microelectronics program. These areas include:

1. Instrumentation
2. Tunnel diode fabrication
3. Thin film studies
4. P-N junction theories and experiments
5. Radiation effects.

Because of the newness of the field, a rapid reorientation has been required of electronics people, which is still going on at NRL, and a considerable effort has been devoted to the design and development of suitable instrumentation and equipment for carrying out the evaporation and processing techniques.

For example, Figure 1 shows a plan view of a multi-stage evaporator designed by Edward Bean of the Electronics Division and constructed in the NRL shops. This device is intended to facilitate the formation of complete electronic circuits in the form of thin films by vacuum evaporation on a single substrate. The first stage is located directly over an off-set pumping port. In this position the substrate surface will be cleaned and out-gassed by a low pressure glow discharge or by a de-focussed electron beam. The substrate may then be advanced one stage at a time above fixed chimney mounts containing two filaments or two boat sources in each stage. Power is


VERTICAL SUPPORT
GLOW DISCHARGE FEED-THROUGH POST
SILICON MONOXIDE STATION
MANIFOLD PUMPING PORT
BELL JAR
DOUBLE FILAMENT STATION
SHUTTER SHAFT ROTARY SEAL
DOUBLE BOAT STATION
FILAMENT FEED-THROUGH POSTS
OCTAL HEADER
SUB STRATE SHAFT PUSH-PULL ROTARY SEAL
SUB STRATE HEATER FEED THROUGH POSTS
COMBINATION STATION

EVAPATROL BASE

Figure 1

supplied through slip rings to wiper contacts which advance from stage to stage along with the substrate. Substrate masks are mounted in floating mask holders on a mask plane and are accurately positioned to the substrate by tapered dowel pins as the substrate holder is advanced to each stage. Seven shutters of the Japanese-fan type are operated in tandem from an external control to protect the substrate from the first out-gassing of the material to be evaporated and to enable deposition to be stopped when the desired thickness has been reached. A controlled substrate heater and means for externally monitoring the temperature and film thickness is provided. It is thus possible to evaporate as many as fourteen different materials without exposure to the atmosphere in a single operation.

Limitations caused by the lack of proper instrumentation have also shown up in our efforts to produce evaporated tunnel diode circuitry. You may recall from our discussion last year that we were particularly desirous of evaporating arrays of tunnel diodes and resistors. Some understanding of why this is so may be gleaned from a comparison of Figures 2 and 3, each of which shows comparable circuitry required to perform a shift register function in equipment of military interest. Figure 2 is a printed circuit board on which is mounted high speed switching-type transistors, condensers, diodes, resistors, inductive resistors, etc. The circuit of Figure 3 contains only tunnel diodes and resistors and yet performs essentially the same circuit function. The savings in cost and gain in simplicity are tremendous and the temptation to try to reproduce the circuit of Figure 3 in thin films is obvious.

Figure 4 shows two stages of a tunnel diode shift register circuit of a well-known type using a three phase clock selected for preliminary experimentation. Figure 5 shows a configuration of resistive and conductive films in conjunction with an array of tunnel diodes to form four stages of a shift register. In this arrangement, a larger number of tunnel diodes can be fabricated on the germanium bars than is actually required to complete the circuit, thus permitting the selection of tunnel diodes which best meet the peak current requirements and increasing the yield of acceptable circuits and also perhaps extending the life of the circuit, at least in laboratory use, by providing redundant components for replacement in case of tunnel diode failures.

We have had no difficulty in forming the resistive components of this circuit using nichrome films deposited at 300°C on polished quartz substrates in vacuum at 10^{-6} torr, and annealed at 400°C before covering with a one-micron-thick film of silicon monoxide to obtain a passivated surface. The conducting lands are formed by first laying down an 800-Angstrom-thick layer of chromium and then covering with a thick layer of gold. This technique greatly enhances the bonding capabilities of lead wires to the film conductors over the use of either metal by itself. At present, the leads are attached to the land areas by low temperature soldering of indium to the thin

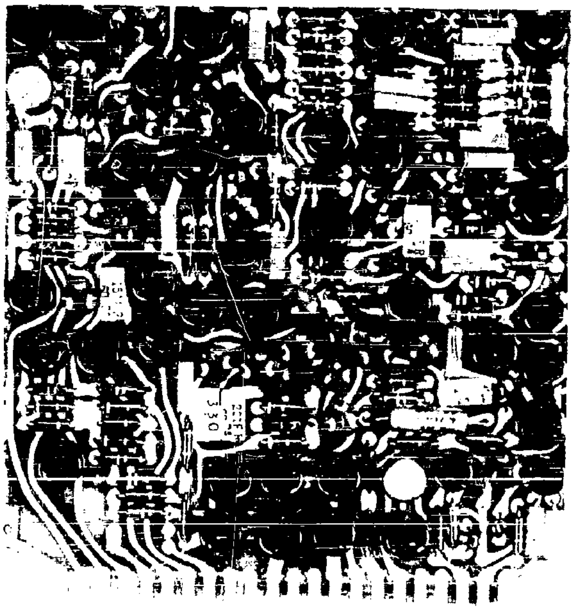


Figure 2

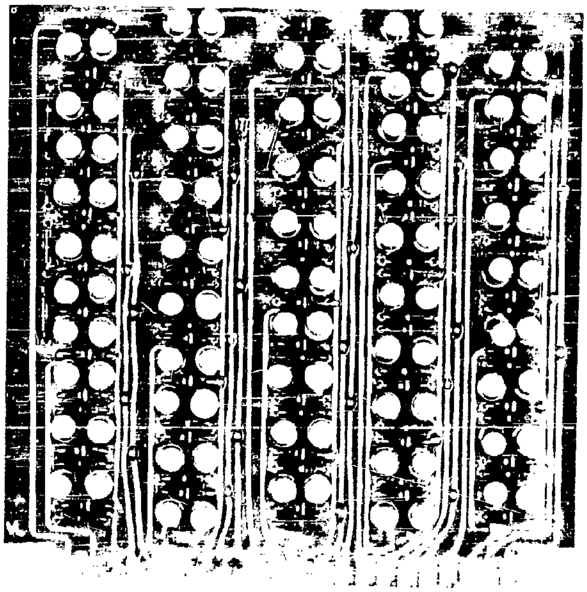


Figure 3

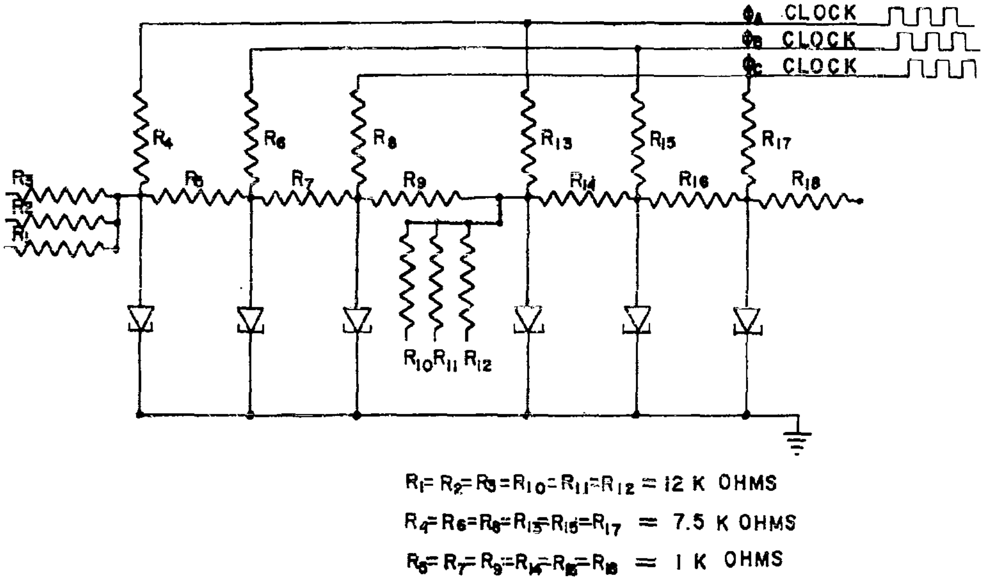

ϕA CLOCK
ϕB CLOCK
ϕC CLOCK
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10 R11 R12
R13
R14
R15
R16
R17
R18
R1=R2=R3=R10=R11=R12 = 12 K OHMS
R4=R6=R8=R13=R15=R17 = 7.5 K OHMS
R5=R7=R9=R14=R16=R18 = 1 K OHMS

Figure 4 - Two States of a Tunnel Diode Shift Register

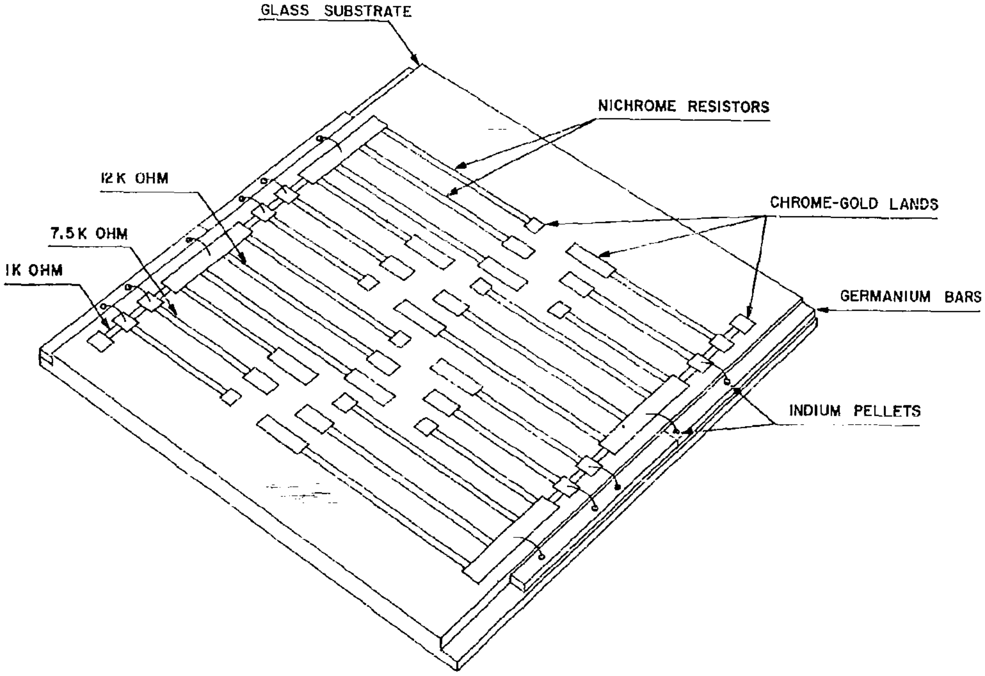

GLASS SUBSTRATE
NICHROME RESISTORS
12 K OHM
CHROME-GOLD LANDS
7.5 K OHM
1 K OHM
GERMANIUM BARS
INDIUM PELLETS

Figure 5 - Four Stages of a 3ϕ Tunnel Diode Shift Register

films; an ultra-sonic welder has been ordered from which better results are expected.

Although we have been quite successful in making tunnel diodes by the alloying-junction technique of indium on N-type germanium outside of a vacuum system, our attempts to evaporate the indium dots did not result in good junctions. Although this is still being investigated, apparently the difficulty results, at least in part, from contamination of the germanium surface by back streaming of oil from the oil diffusion pump. Several approaches, including improved baffling of the pumping system and electron-beam cleaning of the germanium surface just before evaporation of the indium, are being followed.

The Solid State Electronics Branch at NRL is continuing its study of thin semi-conductor films. Considerable success has been achieved in evaporating germanium on amorphous quartz to obtain strongly oriented crystals of germanium, as indicated by both X-ray and electron diffraction patterns. The effects of vacuum-evaporation parameters, such as source temperature, substrate temperature, film thickness, condensation rate, ambient and source material, on the properties of germanium films are being investigated by electron diffraction, electrical and optical measurements. This investigation is being applied to deposition on both amorphous and crystalline substrates. Contamination-conversion effects of bulk germanium in the vacuum evaporation process are also being investigated with the aim of further clarification of the p-character of evaporated germanium films.

Other work is being done in this Branch on the theory of p-n junctions including the effect of injection level on minority carrier lifetime, and the production of unusual capacitance versus voltage laws by variation of the impurity distribution. In particular, Mr. Marinos of this Branch has found a case in which the junction capacitance is proportional to the reciprocal of the junction voltage instead of the usual inverse square root or one-third power. An experimental study of the effect of temperature on Pb-Te p-n junctions made by an alloy process is also being made by this same branch.

One of the basic problems in microelectronics involving the use of thin films is to obtain an adequately-clean substrate, free of contaminants and absorbed gases. A different approach to this problem has been taken by W. H. Vaughan and C. R. Kohler of the Crystal Branch of the Laboratory's Solid State Division. In their technique, large single crystals of rock salt are cleaved under vacuum to produce atomically-smooth planes on which thin films of various metals such as copper, silver, and gold have been evaporated. If desired, these films may be easily stripped off the substrate by immersing in water. The films so obtained are free of pin holes and do not crumple indicating the absence of internal stresses. It seems likely that a sandwich of multiple films could be prepared in this way without the necessity for heat treatment to relieve internal stresses.

Figure 6 shows a drawing of the apparatus for cleaving crystals under vacuum. The movement of a permanent magnet outside the bell jar depresses pin A allowing the cleaving knife to move under the influence of the wound spring and strike the crystal. Figure 7 shows the actual apparatus.

One of the possible advantages of the thin-film approach to microelectronics is the relatively low susceptibility of thin films to the effects of radiation. Various dielectric materials, such as lucite, polyethylene, styrene, polyvinyl, teflon, and mylar films and sheets are being studied to determine the changes in electrical properties resulting from irradiation by high energy particles, such as electrons and protons, and the effects of high electrical fields. Studies in a nuclear radiation field are also planned by the Electromagnetic Materials Branch of the Solid State Division.

The effect on semi-conductor devices of fission neutrons and gamma rays, such as produced by the NRL swimming pool research reactor operating at a one megawatt power level, is being studied by the Security Systems and Avigation Branch of the Electronics Division. This study differs from most previous studies of a similiar nature by including measurements taken while the irradiation was actually taking place as well as before and after irradiation.

Another difference is that the rate of radiation was adjusted so that about thirty hours were required to reach beyond the accepted threshold of damage for semi-conductors (10^{13} neutrons/cm^2) thus avoiding the accelerated testing usually done.

Figure 8 shows the power level of the reactor during irradiation, the ambient temperature inside the experiment container, the d-c forward current transfer ratio for a germanium PNP transistor (2N705), and for a silicon NPN transistor (2N706), as a function of the irradiation time. It can be seen in this figure that there is a large change (25%) in d-c beta of both transistors at about 10^8 neutrons/cm^2 which is well below the previously reported threshold of damage. This observation would have been difficult to detect in a high flux field.

Another significant result is illustrated in Figure 9. Although the germanium transistors suffered almost no permanent damage due to the radiation, they were very much affected during the period of radiation as can be seen from the output characteristics. By contrast the silicon transistors were permanently damaged. Thus, although the frequently-made statement that germanium devices are

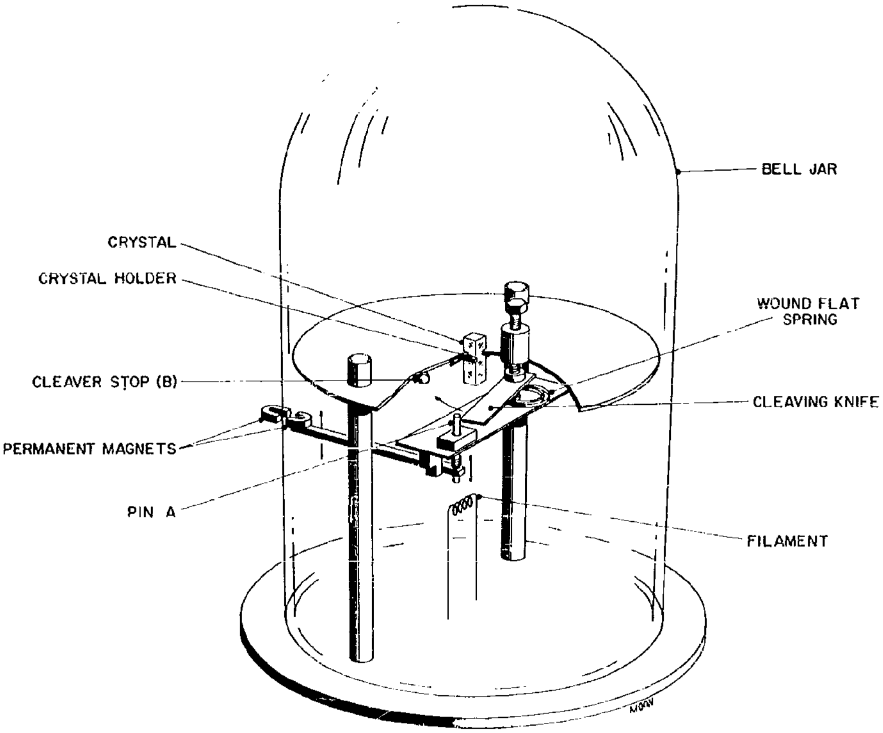

BELL JAR
CRYSTAL
CRYSTAL HOLDER
WOUND FLAT SPRING
CLEAVER STOP (B)
CLEAVING KNIFE
PERMANENT MAGNETS
PIN A
FILAMENT

Figure 6

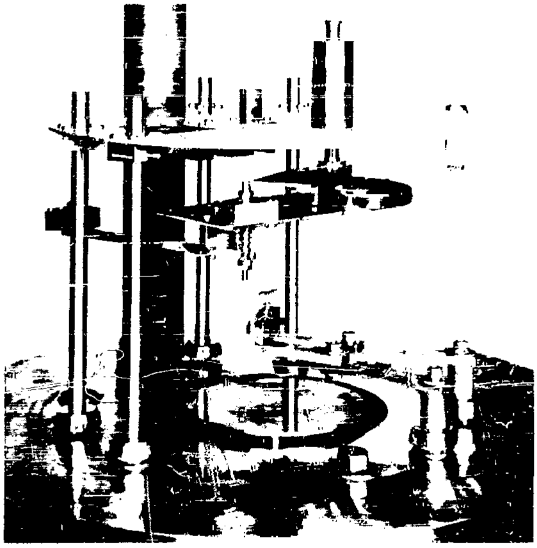


Figure 7

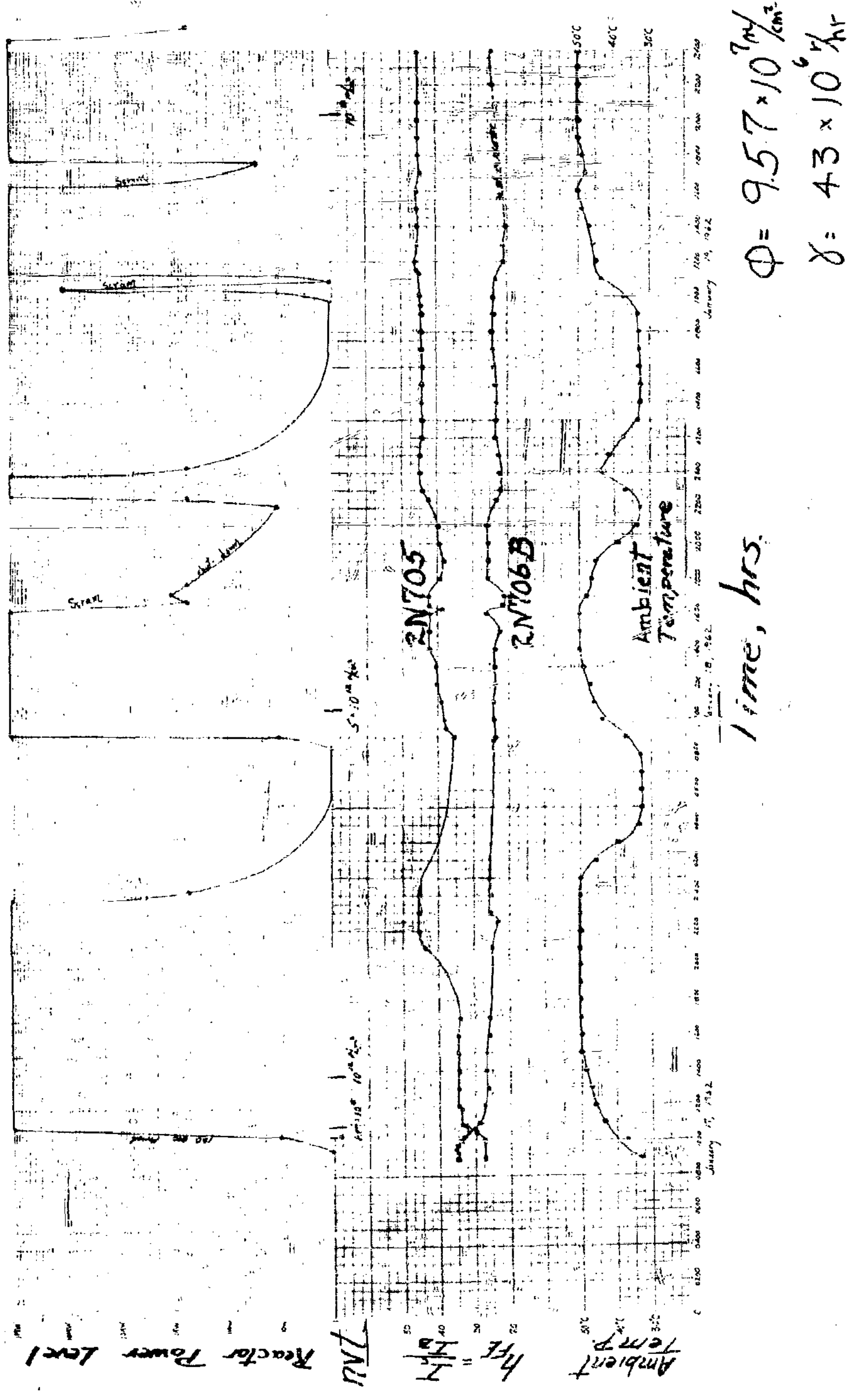

Reactor Power Level
nvt
$h_{FE} = \frac{I_c}{I_B}$
Ambient Temp.
Scram
Scram
Scram
2N705
2N1068
Ambient Temperature
50°C
40°C
30°C
January 17, 1962
January 18, 1962
January 19, 1962
Time, hrs.
Φ = 9.57 × 10^7 n/cm² sec
γ: 43 × 10^6 r/hr

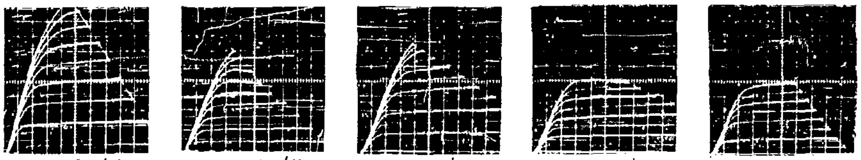
Figure 8

less susceptible than those of silicon is apparently true, it must be qualified to refer to permanent damage. Further studies at still lower flux rates and designed to separate the effects of gamma radiation from those of neutrons are planned.

Dr. Schindler of the Metal Physics Branch of the Metallurgy Division has been studying the effects of neutron radiation on thin films of ferromagnetic materials, particularly nickel ferrite Ni_3Fe. The films were vacuum deposited on quartz substrates held at 100°C and were of various thicknesses between 2800 and 4400 angstroms. The samples were sealed in evacuated quartz tubes and irradiated in the Brookhaven Graphite Reactor operating at 16 megawatts for 504 hours. It was found that, when the films were subjected to a constant magnetic field during the neutron irradiation, a significant change occurred in the uniaxial magnetic anisotropy constant but otherwise not. These studies are continuing.

In summary, it may be said that NRL is continuing to improve its facilities and instrumentation for producing microelectronic circuitry, studying the electrical, optical, and magnetic properties of thin films, and investigating the effects of nuclear radiation on materials and devices of special interest to the field of microelectronics.

2N726 PNP SILICON SWITCHING TRANSISTOR (TI)



a. V = -2ma/div
H = -0.2v/div
I_B = -0.1ma/step
h_{fe} = 28
nvt = 0

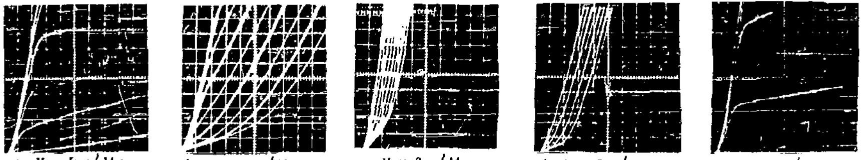
b. V = -2ma/div
H = -0.2v/div
I_B = -0.1ma/step
h_{fe} = 15
nvt = 6.90x10^{12} n/cm^2
reactor shut down

c. V = -2ma/div
H = -0.2v/div
I_B = -0.1ma/step
h_{fe} = 15
nvt = 1.15x10^{13} n/cm^2
reactor at 1 MW

d. V = -2ma/div
H = -0.2v/div
I_B = -0.1ma/step
h_{fe} = 13
nvt = 1.15x10^{13} n/cm^2
reactor shut down

e. V = -2ma/div
H = -0.2v/div
I_B = -0.1ma/step
h_{fe} = 13
nvt = 1.15x10^{13} n/cm^2
reactor shut down
4 months after d.

XN192 NPN GERMANIUM SWITCHING TRANSISTOR (MOTOROLA EXPERIMENTAL)



a. V = 5ma/div
H = 0.2v/div
I_B = 0.5ma/step
h_{fe} = 23
nvt = 10^3 n/cm^2
reactor shut down

b. V = 5ma/div
H = 0.2v/div
I_B = 0.5ma/step
h_{fe} = 20
nvt = 3.76x10^{12} n/cm^2
reactor shut down

c. V = 2ma/div
H = 0.2v/div
I_B = 0.5ma/step
nvt = 5.48x10^{12} n/cm^2
reactor at 1 MW

d. V = 5ma/div
H = 0.2v/div
I_B = 0.5ma/step
h_{fe} = 12
nvt = 8.5x10^{12} n/cm^2
reactor shut down

e. V = 5ma/div
H = 0.2v/div
I_B = 0.5ma/step
h_{fe} = 23
nvt = 8.5x10^{12} n/cm^2
reactor shut down
4 months after d.

Figure 9

U. S. NAVY UNDERWATER SOUND LABORATORY MICROELECTRONICS PROGRAM

S. J. Haefner
U. S. Navy Underwater Sound Laboratory
Fort Trumbull, New London, Connecticut

The Underwater Sound Laboratory continues to monitor the microelectronics research and development work in progress at government and commercial establishments. As an observer, I should like to comment that microelectronic techniques and devices are coming along at a much faster pace than I anticipated only a few years ago.

The electronic requirements of space satellites and missiles have been a major factor in accelerating this work. In addition, the research and development microelectronics programs of ONR and BUSHIPS undoubtedly payed an important part.

There is much more to be done however before introduction of microcircuitry into the fleet electronic equipment. For example, the Committee on Undersea Warfare, in their January 1962 report on Naval Electronics, points out that the process of establishing the relative merits of the various techniques to attain high reliability will be an expensive process and may require a substantially higher level of military support than the early development activities have required.

To quote from the report, "It is important that these advanced techniques not be allowed to enter the fleet prematurely. Such an occurrence could delay the realization of much of the potential value of microelectronics by complicating logistics, by leading to too early a widespread use of techniques insufficiently developed, and by early failures that may not be readily corrected within the existing structure of the fleet."

It is interesting to note that the Army is making an intensive effort to incorporate micromodules into all appropriate army equipment. Eight million dollars has been allocated for Fiscal '63, double the amount for the previous year. It was stated that integrated circuits would be the ultimate type of micromodule when the cost and reliability factors have been ironed out in the still distant future.

MICROELECTRONICS FOR GENERAL SHIPBOARD USAGE

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U.S. Naval Material Laboratory
Brooklyn 1, New York

The Material Laboratory is concerned with the adaptation of microelectronics to General Shipboard Electronics, wherein circuitry is pre-dominantly of the analog variety. As we saw this task, it was felt that the more important facets of this problem were:

a. availability of microminiature circuitry suitable to current shipboard requirements.

b. the necessity to generate 'high production' yields with low unit costs and relatively low volume of required spares: This assumption being contingent upon standardization of general use functions suitable for use in a wide variety of shipboard equipment.

c. suitability from a maintenance viewpoint-this being a function of rapid identification of faulty modules and convenient operational surveillance without the need of extensive technical training or elaborate test gear.

d. development of assembly techniques which would permit ready removal and replacement of modules. (When properly defined, such a procedure would also permit the adoption of new miniaturization techniques to current equipments while obviating the necessity for major field changes to the equipment with each evolutionary advancement).

We have, during the past year, moved simultaneously along multiple paths in order to arrive at some answers to these problems. Although we have not yet arrived at positive recommendations, we have made progress in the following areas.

First - The Availability of Analog Circuitry in Microminiature Form.

This was explored through requests for proposed bids on eleven functional circuits. Requests were sent to 24 of the most prominent manufacturers in the field: seven submitted proposals for accomplishing the desired task; two have indicated that proposal are forthcoming. Eight have replied, indicating inability to produce the circuits or a general lack of interest under present state-of-the-art achievements. Of the seven proposals received, five were "discrete component" types and two were hybrid (thin film and discrete components). One manufacturer of "molecular blocks" indicated that their process at the present time would not lend itself to the support of this program. This appears to be the concensus of other manufacturers engaged in developmental studies employing this technique.

Second - Standardization of Module Function.

The eleven circuits used in the availability inquiry were selected from among 24 circuit functions determined by Vitro Corporation to exist in approximately 60% of all general shipboard equipment. Re-engineering of standardize forms of these circuits, generated by Vitro Corporation,were accomplished after development and fabrication of a Video Amplifier which is used in the AN/SPS-28 Radar System: this step was taken to evaluate and improve the effectiveness of fault location and operational surveillance techniques when functional module are employed. Each of the circuit functions were standardized with respect to input, output, and transfer characteristics and power supply requirements. The transfer characteristics (input and output impedance) were set to permit compatible interchangeability of similar "black box" functions which may be manufactured by diverse methods and to be amenable to variations in input and output loading. A list of the eleven functions considered in this program are contained in addendum 1.

Third - Module Configuration Standardization.

In order to obtained maximum response from the manufacturers contacted in this inquiry, no restrictions were placed on the configuration a completed circuit module might take; however, we expect from studies underway that a useful compromise can be made with respect to modular dimensions. These studies include: (a) development of a "standard time signal" radio receiver using the RCA modular concept. Each functional module not available from RCA will be designed and fabricated at MATLAB. (b) A third generation development of the Video Amplifier, previously mentioned, is in the planning stage - the second generation Video Amplifier is nearing completion: the latter equipment utilizes standard transistor module, which are also being standardized under the Modular Assembly program. These studies lead to the following tentative conclusion:

1. We are reasonably sure that equipments, requiring as many as 24 functional module, can be built into a unit about 8" X 2" X 2": complete with power supply, monitoring facilities and test points. This, we expect, can be achieved without introducing problem of cooling, module interference and accessibility. This applies to equipments exclusive of display outputs which are inherently not amenable to microminiaturization.

2. Looking a bit deeper, a "one foot square by one inch" deck can easily accommodate 500 functional modules (representing up to 5000 or more parts in conventional circuitry) having readily accessible maintenance features and no difficult problems of cooling. For larger equipments, several decks could be employed, holding several thousand functional modules (with up to the equivalent of 10 components each) in one cubic foot of space.

Fourth - Maintainability of Modularized Equipment

In determining details of micro-assembly techniques we have relied on the experience of experimentation obtained during the development of prototype equipments which utilize conventional functional modules: in so doing we have concluded that the only "test points" required for in-service examination of expendable modules (highly characteristic of micromodules) are the basis input and output functions: these "test points" along with a simple (but effective) current monitoring system for each module (which indicates a "go-no go" condition) is the most expedient means for rapid surveillance and maintenance of equipments which utilize this concept of design. We hope to verify these concepts through development of various representative naval equipment.

Fifth - Effectiveness of Function Standardization

The 24 standardized functional circuits previously mentioned were evolved by Vitro Corporation as being representative of 30% of the total electronic functions which were found in a survey of 84 equipment types. Each of these functions were found in approximately 60% of all equipments surveyed: further investigations revealed that 80% of the equipments which contained these functions could employ standardized modules.

A cursory examination of electronic equipment aboard a modern aircraft carrier revealed eight systems (such as radar, sonar and communications) comprising a total of approximately 120 types of equipment. Each of these equipments contain an average of 20 functions: approximately 60% of these functions can be microminiaturized. It has not yet been determined as to what percentage of these functions can be standardized, however, on the basis of the Vitro report, it is believed that 30% is a reasonable estimate.

Conclusion

In consideration of the foregoing, we believe that the time is ripe for the development and installation of some of the shipboard equipments utilizing modular construction which employ the best current techniques of microminiaturization. These pilot installations would be instrumental in providing background information on the many field problems of fleet operation and maintenance, and could well establish the validity of these concepts in future equipment designs.

The program that I have just outlined is considered absolutely necessary as a prerequisite to achieving a large "production-quantity" base required for low initial cost, broadly based maintenance techniques, reliability assurance methods, and low volume of spare parts.

Addendum I

Following are the functional circuits submitted to various manufacturers in a request for bids on limited production utilizing these present "state-of-the-art" techniques.

1.	Audio Frequency Generator	EA2C615E01T
2.	Servo Amplifier	EA2C225E01T
3.	Low Level Limiting Amplifier	EA2C274D01T
4.	Current Deflection Amplifier	EA2C282E01T
5.	Distribution Amplifier	EA2C274D04T
6.	Audio Voltage Amplifier	EA2C213D01T
7.	Audio Power Amplifier	EA2C223E01T
8.	Gated Saw tooth Generator	EA2C374D01T
9.	Single Swing Blocking Oscillator	EA2C374D02T
10.	Monostable Multivibrator	EA2C372D01T
11.	Low Level Mixer	EA2C214D01T

The Microelectronics Program at NEL--A Progress Report

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INTRODUCTION. Much effort is being devoted, both by Laboratories and industrial manufacturing organizations, to the development of techniques for fabrication of microcircuitry in one form or another. Considerably less effort is being devoted to the problem of adapting these devices to large-scale system use or to investigation of many of the basic design considerations--such as, heat dissipation, shielding, power supplies, interconnections, etc.--which are controlling factors in many applications.

It is difficult, if not impossible, to analyze separately the problems in these areas, as the solutions are seldom independent and usually result in an over-all performance compromise in one area to achieve needed performance in another. In effect, then, it is the over-all system which must control the characteristics of component microsystems.

Since the establishment of the microelectronics program at NEL, our effort has been heavily application-oriented with particular emphasis on the problems of using microcircuitry in equipments and systems--particularly computer systems. Part of the reason for this was the fact that our own initial competence lay more in these areas. In addition, however, we felt that there was no way other than direct contact and usage, to gain a true picture of the state of the art in this field. Hence, we have undertaken several investigations, results of which we hope will bring the Navy a few steps closer to extensive utilization of microelectronics in some of the areas where significant pay-offs may be expected.

"P" TIME COUNTER. One of our first application efforts was the implementation of the "P" Time Counter in an NTDS Detector-Tracker Console. The circuit consists of four flip-flops, eight emitter-followers and the necessary control logic as shown in Figure 1. Our functional implementation of this circuit used the RCA Micromodule approach starting with the various wafer components and building up the modules as required by interconnection via the risers. Each module was then encapsulated in an epoxy potting compound which cures at room temperature with a low exothermic reaction. A flip-flop built in this fashion is shown in Figure 2. A very considerable reduction in the over-all counter volume was achieved as will be seen in Figure 3 which shows the "P" Time Counter in conventional form as compared with the Micromodule implementation.

Actually no attempt was made to achieve high-density packaging on a level beyond the Micromodule itself, as we wanted to replace the conventional "P" Time Counter cards directly in a Detector-Tracker Console with the Micromodule implementation. Replacement cards, which are shown in Figure 4 have been in operation in this console for several months with no failures nor even a hint of marginal operation.

From our experience we would conclude that once the Micromodules are fabricated and initially tested, they are quite reliable--provided, of course, that the circuit design itself is not marginal. Difficulties which we did encounter were mainly a function of inferior component wafers which seem to be the result of faulty quality control procedures in RCA's own organization or among its suppliers.

AN/UYK-1 INVESTIGATIONS. We undertook investigation into some of the problems which might be associated with implementation of a logic portion of the AN/UYK-1 with off-the-shelf integrated microcircuitry. The AN/UYK-1 is a medium-size, medium-speed, programmed logic machine.

Because of the nature of the logic in the AN/UYK-1 and in order to limit the extent of the investigation, we chose to reproduce functionally the so-called State Counter. This is shown in block diagram form in Figure 5. Our first effort was to reproduce the functions of this State Counter using Fairchild Micrologic elements in TO-5 headers. The results of this implementation are shown in Figure 6. Similarly the State Counter was reproduced using TI Series 51 Solid Circuits, as well as PSI and General Instrument integrated circuits.

Results of these investigations indicated that for this particular application the Fairchild elements performed beautifully and were far faster than was really necessary. The same was true to some extent of the PSI and the General Instrument elements. The TI integrated circuits were marginal in operation even at the 330-kilocycle operating speed of the AN/UYK-1 and the AN/UYK-1 clock pulse had to be widened by pulse stretching circuitry in order to achieve even satisfactory operation because of the slow rise times of these TI elements.

In each case, level changers were used in order to drive the micro-circuit State Counters with the same information used in the AN/UYK-1. This turned out to be something of a surprise as the operation of the logic at the 0 and 3-volts levels (rather than the 0 and 12-volt levels of the AN/UYK-1) gave no trouble at all even in the presence of ambient noise. Furthermore, in the case of the Fairchild Micrologic elements, the design was so conservative that both the signal levels and the supply voltages could be varied over quite a wide range from the nominal values without disturbing their good solid operation. To a considerably lesser extent this was true of the other integrated circuits as well.

In addition to implementation of the State Counter, we built an RS Flip-Flop with Fairchild elements which, together with appropriate level changers mounted on a standard AN/UYK-1 card, was used to replace the RS Flip-Flop cards in numerous locations in the actual machine. These worked very nicely but, like the State Counter, would hardly be a practical solution in a full-scale functional replacement in the AN/UYK-1. In other words, if the machine were largely rebuilt using integrated circuitry, level changers on the individual cards in connection with individual circuits would not be necessary.

Realizing that our conclusions were based on a somewhat limited investigation, we felt that a more massive implementation of logic using integrated circuitry of the type described above, would be desirable. For this purpose we built a shift register using 81 of the Fairchild Micrologic elements packed tightly on a 4" x 4" card and operating at a $2\frac{1}{2}$ megacycle clock rate. The logic block diagram of this shift register appears in Figure 7. To date this has disclosed no unusual problems in interconnection, heat dissipation, cross-talk, noise or other system-type considerations.

MICROMODULE TEST SET. In order to examine more closely the advantages and problems of an integral unit fabricated entirely of microcircuitry, we contracted with RCA for fabrication of a system interface Test Set to be built to our design. The function of this test set, which operates in any one of four modes, is to allow static or dynamic examination of the condition of each of 30 parallel data lines carrying information from one portion of a large digital system to another. Heretofore we have carried out this function in a somewhat painful manner using either a line by line procedure with a Tektronix scope or by building limited special-purpose test equipment to examine a few lines at a time. The RCA Test Set, which is approximately 10" x 5" x $7\frac{1}{2}$" and weighs nine pounds, including built-in rechargeable batteries, is built entirely of 94 Micromodules and is shown in outline form in Figure 8. A block diagram of the test set is shown in Figure 9. The physical construction and the component package is shown in Figure 10. We expect this portable device to be extremely useful in examining problems at the interfaces of large-scale data systems and we expect to gain some experience as to the reliability, ease of replacement, and operational characteristics of Micromodules.

B-D CONVERTER. In order to study a few more of the system-type problems of microelectronics, we have designed a binary-to-decimal converter and readout which will be used to sample and display useful information in a real-time data system. Figure 11 is a block diagram of the logic of this converter. A large part of the converter is being built of small conventional components using welded cordwood construction potted into convenient modules. The shaded part of the logic, however, which is repeated several times (once for each digit) is being built in six different ways. An identical circuit in the operating unit is being functionally reproduced using one pellet approach, three different thin-film approaches, and one integrated-circuit approach.

The pellet implementation is being carried out for us by General Dynamics (Astronautics) using two basic circuits, a flip-flop and a gate and inverter as shown in Figure 12. These circuits are packaged in a physical configuration similar to that shown in Figure 13. The substrate is an epoxy-paper material. The pellets themselves, which are each 0.1" in diameter, are interconnected by means of Hysol Ag epoxy deposited in the grooves and fired at 200°F. Resistors are a rather complex Cermet.Capacitors use barium titanate dielectrics. Diodes are the equivalent of 1N914's; and transistors are equivalent to 2N1258's.

One of the more unusual of the thin-film approaches is being implemented by IBM (Kingston) using a batch process in which 56 simultaneously-deposited thin-film circuits are placed on a substrate $2\frac{1}{2}$" x $3\frac{1}{2}$". Each circuit on the panel is a TRL NOR circuit, which through the use of film interconnections can be arranged to provide any desired computer function. Aside from the transistors, which are separately attached 2N744's, three basic materials are used for the formation of the thin-film passive elements and interconnections. Resistors are Cermet (chromium-silicon monoxide mixture); conductors are chromium-copper; and insulators are silicon monoxide. Seven stages of the converter can be placed on one of these integrated thin-film panels using the logic of Figure 14. Two panels such as the one shown in Figure 15 will thus provide the required 10 positions plus four spares. Logic levels are 0 and 6 volts.

The integrated circuit approach by Westinghouse makes use of a double-NAND gate as the basic logic element from a combination of which any desired logical function can be performed. Three basic packages, a gated flip-flop, a five-input AND gate plus inverter, and a clock inverter, are used for implementation of each of the 10 bits as shown in Figure 16. The transistors, resistors and diodes of the basic circuit are formed by a triple diffusion process into silicon. Figure 17 is a photograph of a batch of these NAND gates on a single wafer. Two of the double-NAND gates are then mounted in a special 12-pin header in a manner shown in Figure 18.

With the exception of some work which Bell Labs has reportedly done along these lines, this is the first instance of which I am aware in which the same circuit has been intentionally fabricated in several different ways. The completed converter should provide us with an excellent vehicle for examination, study, and comparison of the physical, electrical and operational problems associated with some of the best fabrication technique work of which we are aware. Perhaps more important, we will be making these observations in terms of an operating physical system of some considerable functional size as contrasted to bench performance tests.

MOCC COMPUTER. One of the first large-scale non-linear applications of integrated circuitry may be in the logic of the CP-667(XN-1)UYK computer for the Mobile OPCON Centers. This is a computer using 10-megacycle logic, for the most part diode-resistor gates and transistor-resistor inverters. The comparatively few basic structures that appear to be necessary can be diffused into silicon chips as shown in Figure 19 and packaged in TO-5 headers. Some 8,000 of these cans would be used in one computer in which the basic module would likely be three cans mounted on a card approximately the size of an existing AN/USQ-20 computer card. We have been working with RRU, Motorola and the Bureau of Ships to this end.

ASSOCIATED DISCIPLINES. As we continue our work with microelectronics it becomes more and more evident (particularly from the system point of view) that the interplay of several associated disciplines will be necessary in order fully to exploit the potential advantages of the microelectronics art. For example, the type of logic elected for use in any particular application has a very material affect, not only on the ease with which the functions can be performed using microelectronic modules, but also on the number of basic circuits which will be required, the ease with which these circuits can be fabricated, etc. This is not necessarily to suggest the actual design of microelectronic logic circuitry need be performed by someone other than the circuit design engineer, but he must certainly have a good appreciation of the problems and limitations of the type of microcircuitry which he proposes to use.

Another equally important function which can be served well by microelectronics is the question of redundance for the purpose of automatic fault location and repair. The obvious weight and space saving aspects of microcircuitry make possible the consideration of some form of redundance which can serve many purposes, not the least of which is the possibility of automatically replacing a circuit which has been determined to be faulty until such time as the original circuit can be repaired during a period of low demand level upon the system. This is the so-called "automatic repairman" function which is being probed by a few organizations. In addition, as was suggested at our last meeting, the question of new and more powerful logics and programming techniques immediately suggested by the possibility of large populations of logical elements in comparatively small volumes. Such effort would benefit considerably from the practical point of view by an understanding of the peculiarities of the various types of microcircuitry being considered.

Neither should we feel that this interplay is peculiar to computer-type circuits. It is certainly true that considerable benefit might be derived from some effort to invent new circuits in the linear amplifier field rather than attempt to warp the existing designs to the extent that they can possibly be fabricated with state-of-the-art techniques.

PROBLEM AREAS. Despite considerable progress in the microelectronics field, not only in technology of fabrication but in the application of the devices themselves to perform useful electronic functions, some of our basic problems still remain largely unsolved--especially when one considers them in the aggregate in terms of any one type of device or microelectronic approach.

Packaging, for example, remains a problem on the substrate level (including the question of passivation versus hermetic sealing) as well as on the larger module level. The question of interconnections on the module level may well cancel the gains on the substrate or chip level. Consideration of heat dissipation problems on an equipment or system level quickly puts an end to many numbers games that are played entirely with mythical component densities. It is true that new approaches such as evaporative cooling, in which whole electronic assemblies are immersed in liquid, may hold some of the answers to this problem.

Although we recognize some of the effects of either steady state or pulsed nuclear radiation on electronic circuitry, some of the very materials that are most useful from a functional point of view are most susceptible to damage from this radiation.

The question of how to standardize, what to standardize, and in some cases even whether or not to standardize, in microelectronics, is still the subject of very active arguments in industry groups as well as in government. It begins to appear that some standardization, at least of form function or interconnection, may not only be possible but desirable within the near future in certain forms of microcircuitry such as the header packages. The question of reliability is still largely an unknown and unproven factor without really significant experience data on operating circuits in a system environment to back the claims.

The point is that mutually compatible solutions to these and other problems are required in the same approach or form of microcircuit for truly satisfactory microsystem electronics. It is evident that considerable work remains to be done.

EIA. For the past six months I have been associated with the Microminiature Components Advisory Committee (MCA) of the Electronics Industries Association as the Naval representative. MCA is divided into two working sub-committees, MCA-1 on Basic Components and MCA-2 on Integrated Components. These are essentially users' groups and as such wrestle with such familiar problems as nomenclature, packaging, connectors, electrical characterization, standardization, etc. One of the most useful documents which has come out of MCA recently is their recommended nomenclature and definitions in the microelectronics field which they hope will be adopted by EIA for uniform use throughout the industry, thereby relieving some of the present widespread semantic confusion. It is interesting to note that this list does not contain the word "microelectronics", but rather refers to the general subject as microsystems electronics in accordance with the precedent established by the IRE and AIEE.

The membership of MCA represents a broad cross-section of the industrial organizations active in the field and because of this, both their meetings and their reports offer a ready means of periodically sampling the pulse of the industry on numerous aspects of microelectronics. These people are avidly interested, of course, in definition by the military of its needs in all areas of microelectronics but until such definition is forthcoming they are attempting to organize among themselves a more unified approach to solution of their and our common problems.

PLANS. While we plan to explore more fully some of the above problems and their impact on specific microelectronic implementations, we hope also to delve more deeply into some of the fundamental techniques of fabrication. For this purpose we plan to procure a modest thin-film facility which will enable us to study and thereby gain a better understanding of some of the problems of this type of circuit fabrication.

We hope also to merge to some extent our effort in microelectronics with that in automatic fault location in large-scale systems to study the possibilities of implementation of self-healing techniques of the type mentioned above.

Finally we plan to continue to push the application of microelectronics to larger and more complex circuits and equipments to hasten the availability of reliable microsystems where needed in fleet electronics.

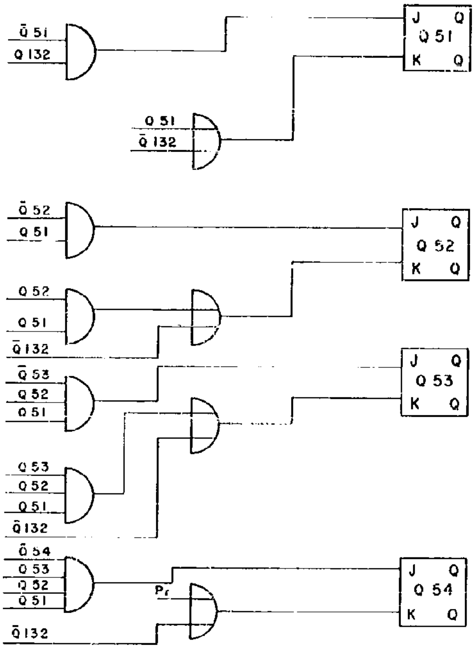

$\bar{Q}$ 51
Q 132
Q 51
$\bar{Q}$ 132
J Q
Q 51
K $\bar{Q}$
$\bar{Q}$ 52
Q 51
Q 52
Q 51
$\bar{Q}$ 132
J Q
Q 52
K $\bar{Q}$
$\bar{Q}$ 53
Q 52
Q 51
J Q
Q 53
K $\bar{Q}$
Q 53
Q 52
Q 51
$\bar{Q}$ 132
$\bar{Q}$ 54
Q 53
Q 52
Q 51
Pr
$\bar{Q}$ 132
J Q
Q 54
K $\bar{Q}$

Figure 1 - Logic for "P"
Time Counter

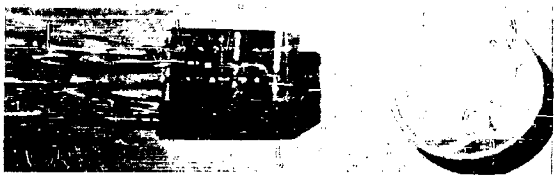


Figure 2 - Micromodule Flip-Flop

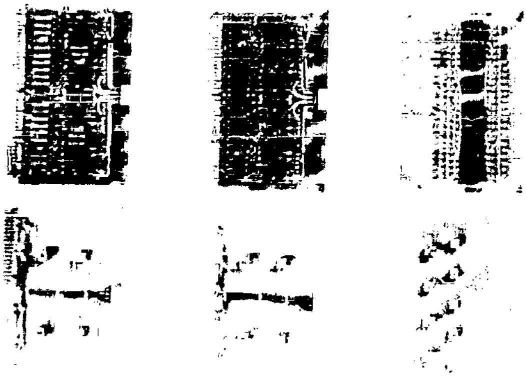


Figure 3 - Comparison of Micromodule
and Conventional Circuitry

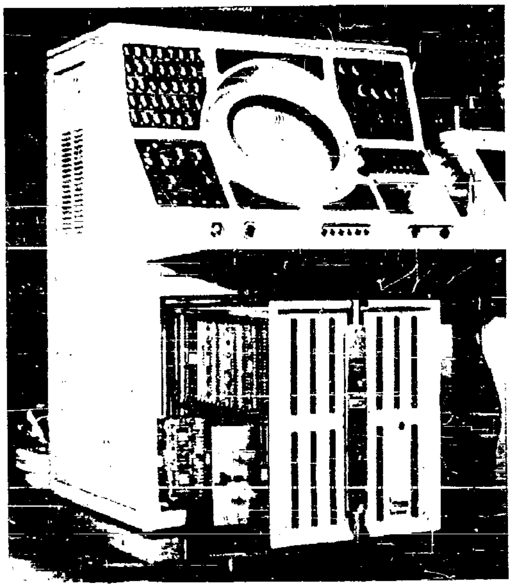
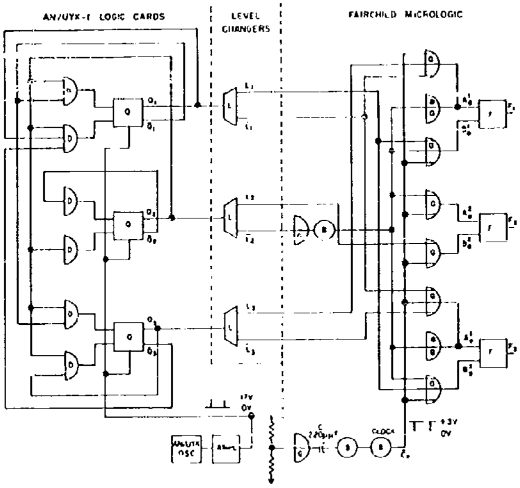


Figure 4 - Micromodules in DTS Console



AN/UYK-1 LOGIC CARDS
LEVEL CHANGERS
FAIRCHILD MICROLOGIC
CLOCK
OSC
+3V
0V

Figure 5 - Block Diagram of State Counter

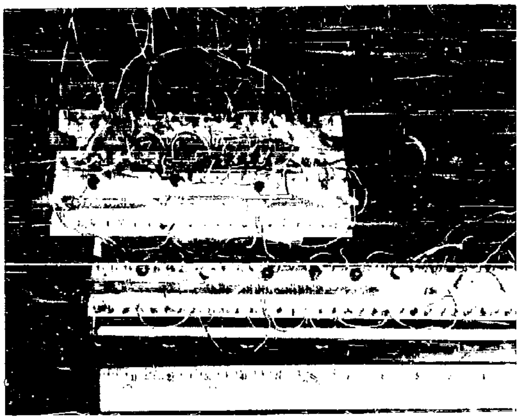


Figure 6 - Fairchild Implemented State Counter

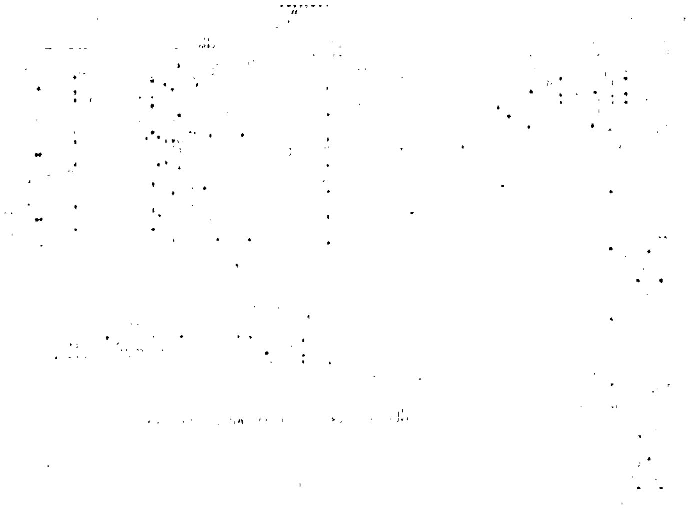


Figure 7 - Eight Bit Shift Register

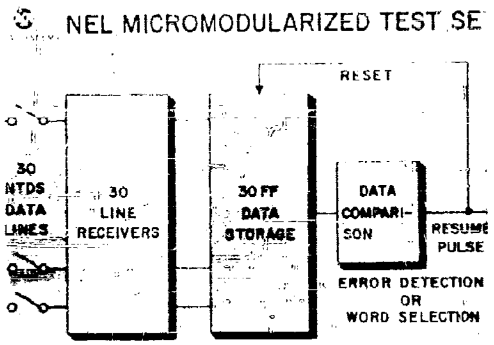

NEL MICROMODULARIZED TEST SE
RESET
30 NTDS DATA LINES
30 LINE RECEIVERS
30 FF DATA STORAGE
DATA COMPARISON
RESUME PULSE
ERROR DETECTION OR WORD SELECTION

Figure 8 - Block Diagram of RCA Test Set

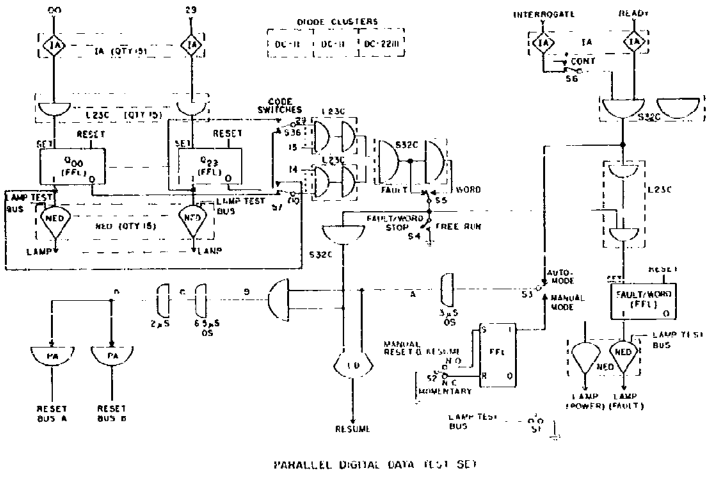

00
23
IA
IA (QTY 15)
DIODE CLUSTERS
DC-11
DC-11
DC-22III
INTERROGATE
READY
CONT
S6
L23C (QTY 15)
CODE SWITCHES
S36
RESET
SET
Q00 (FFL)
Q23 (FFL)
S32C
L23C
FAULT
WORD
S5
LAMP TEST BUS
NED
NED (QTY 15)
LAMP
FAULT/WORD STOP
FREE RUN
S4
S32C
AUTO-MODE
MANUAL MODE
S3
RESET
FAULT/WORD (FFL)
LAMP TEST BUS
2μS
6.5μS OS
3μS OS
MANUAL RESET & RESUME
N.O.
N.C.
MOMENTARY
FFL
PA
PA
RESET BUS A
RESET BUS B
LD
RESUME
LAMP TEST BUS
S1
LAMP (POWER)
LAMP (FAULT)
PARALLEL DIGITAL DATA TEST SET

Figure 9 - Detailed Block Diagram of RCA Test Set

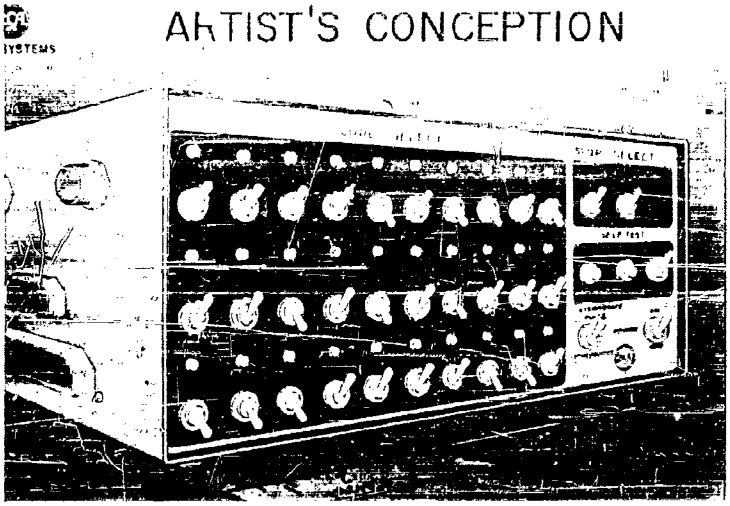

ARTIST'S CONCEPTION
SYSTEMS
STOP SELECT
SELF TEST

Figure 10 - Component Package of RCA Test Set

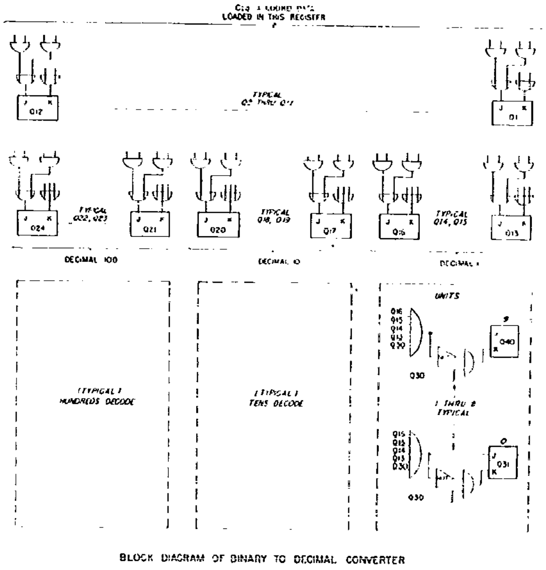
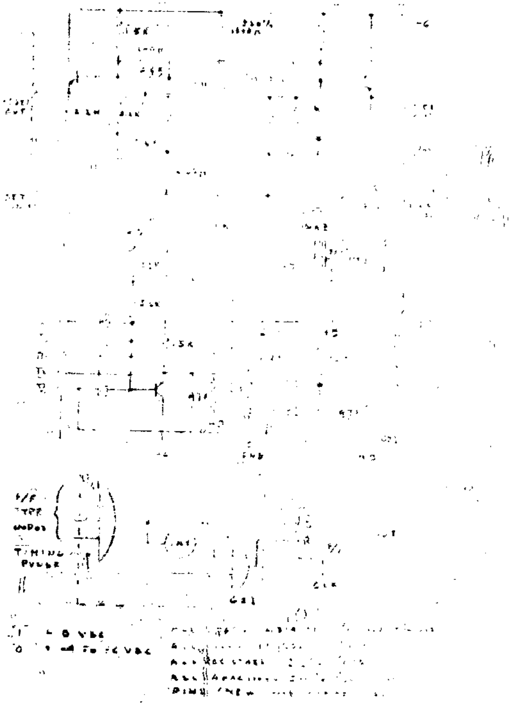

LOADED IN THIS REGISTER
TYPICAL
J
K
Q12
D1
Q24
TYPICAL
Q22, Q23
Q21
Q20
TYPICAL
Q18, Q19
Q17
Q16
TYPICAL
Q14, Q15
Q13
DECIMAL 100
DECIMAL 10
UNITS
Q16
Q15
Q14
Q13
Q30
Q40
9
(TYPICAL)
HUNDREDS DECODE
(TYPICAL)
TENS DECODE
1 THRU 8
TYPICAL
0
Q31
BLOCK DIAGRAM OF BINARY TO DECIMAL CONVERTER

Figure 11 - Block Diagram of B to D Converter

Figure 12 - General Dynamics Circuit of Decade for B to D Converter



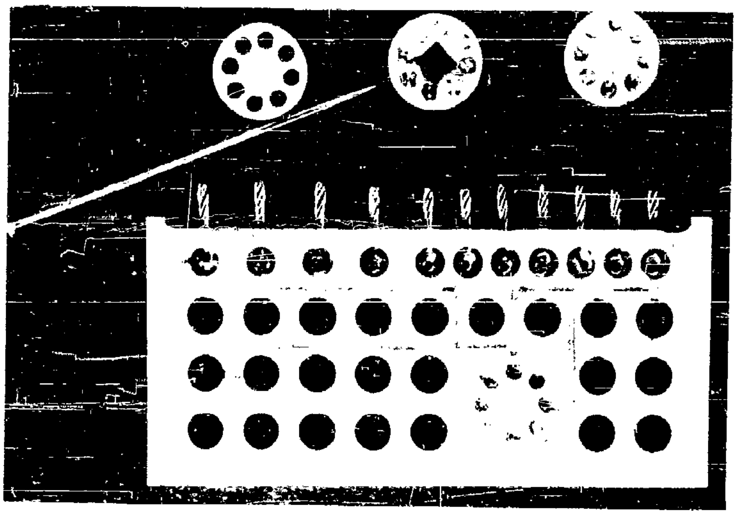


Figure 13 - Pellet Circuitry

Figure 14 - Block Diagram of IBM Thin-Film Circuit

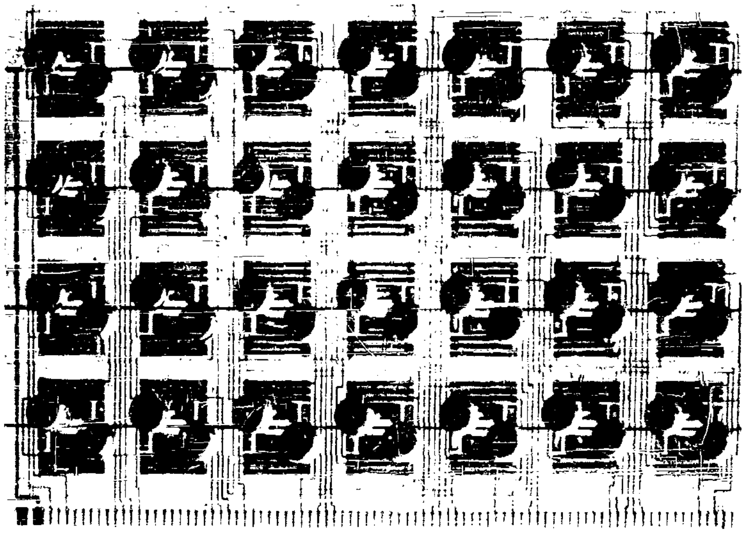


Figure 15 - IBM Thin-Film Circuit

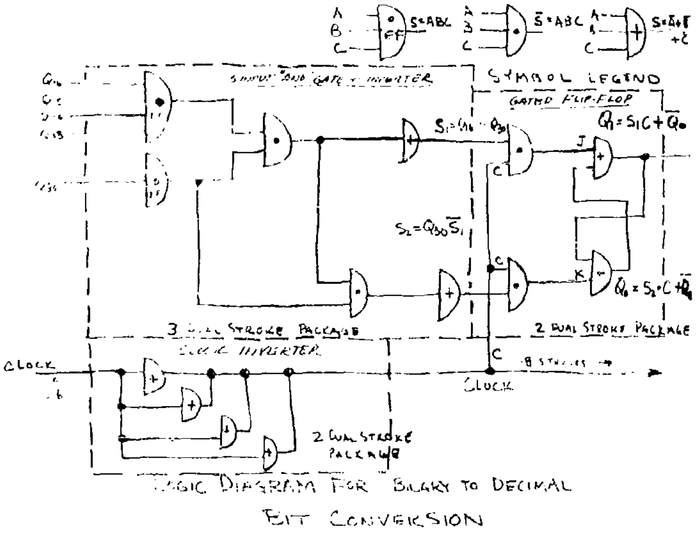

A
B
C
FF
S=ABC
$\bar{S}$=ABC
S=$\bar{A}$+$\bar{B}$+$\bar{C}$
SYMBOL LEGEND
3 INPUT AND GATE & INVERTER
GATED FLIP-FLOP
$Q_1=S_1C+\bar{Q}_0$
J
K
C
$S_2=Q_{30}\bar{S}_1$
$Q_0=S_2 \cdot C+\bar{Q}_1$
3 DUAL STROKE PACKAGE
2 DUAL STROKE PACKAGE
CLOCK INVERTER
CLOCK
2 DUAL STROKE PACKAGE
LOGIC DIAGRAM FOR BINARY TO DECIMAL BIT CONVERSION

Figure 16 - Block Diagram of Westinghouse Integrated Circuits

Figure 17 - Westinghouse Integrated Circuit Wafers

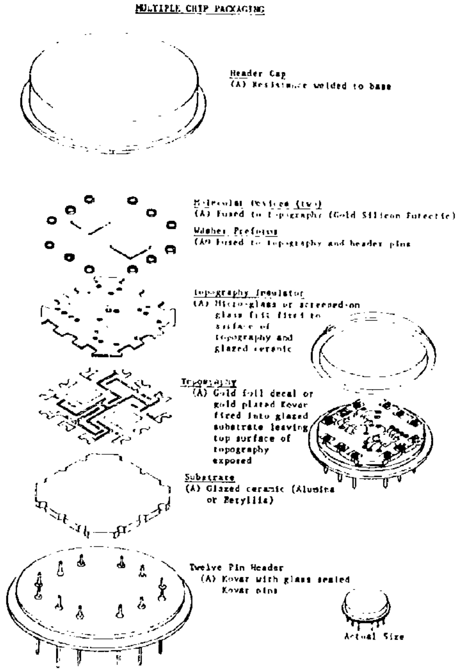

MULTIPLE CHIP PACKAGING
Header Cap
(A) Resistance welded to base
Molecular Devices (two)
(A) Fused to topography (Gold Silicon Eutectic)
Washer Preforms
(A) Fused to topography and header pins
Topography Insulator
(A) Micro-glass or screened-on glass frit fired to surface of topography and glazed ceramic
Topography
(A) Gold foil decal or gold plated Kovar fired into glazed substrate leaving top surface of topography exposed
Substrate
(A) Glazed ceramic (Alumina or Berylia)
Twelve Pin Header
(A) Kovar with glass sealed Kovar pins
Actual Size

Figure 18 - Westinghouse Double-NAND Circuit Mounting

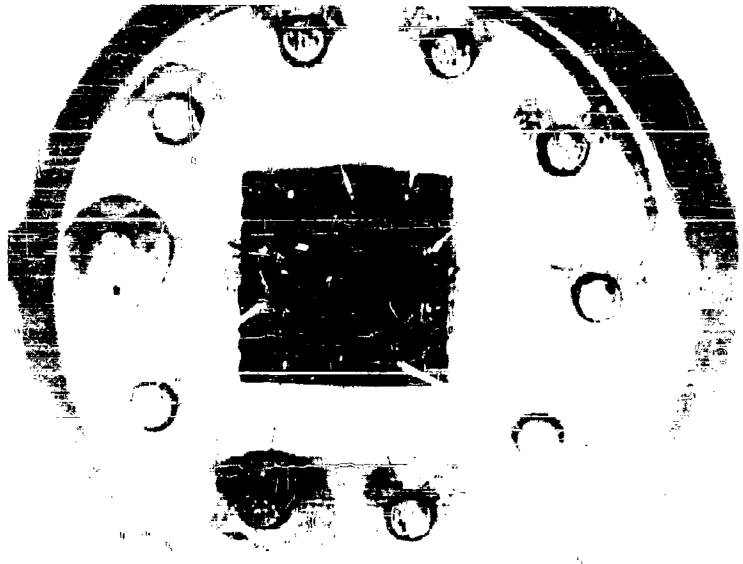


Figure 19 - Motorola Integrated Circuit Wafer

CONTRACTOR REPORTS

Chairmen: Morning Session
Capt. S. F. Balaban, USN
Office of Naval Research

Afternoon Session
L. Schlesinger
Bureau of Naval Weapons

Department of the Interior
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WELCOMING REMARKS

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Assistant Chief for Research
Office of Naval Research

First, I would like to convey the deep regrets of Admiral Coates, Chief of Naval Research, that he could not be here today. He had been looking forward to attending this conference, but urgent business has called him elsewhere. He asked me to express his welcome to you to this meeting on microelectronics, a subject which he considers one of the most important new areas of research with which the Navy is concerned.

The Office of Naval Research is pleased to sponsor this conference, one of a number of scientific meetings and symposia we sponsor as an important avenue for encouraging and promoting new ideas. It has been our experience that a scientist or engineer is able to pick up more late news about research progress in his particular field at a meeting of like interested people than he can glean from sifting the various scientific journals or the mass of abstracts available to him. In a field as new as microelectronics the scientific conference is an especially important and timely source of information as to what is going on in his field.

Microelectronics has been called a breakthrough in the evolution of methods of fabricating electronics equipment. It promises to be a breakthrough in the general trend toward improved reliability, smaller size and lower power dissipation. Microelectronics is based on the exploitation of a greatly expanded knowledge of the physics of the solid state, which may be said to have begun with the discovery of the transistor.

As one would expect, industry has played and will continue to play a major role in pushing this evolution. As one industry report on electronics published a year ago noted, "the exacting requirements for performance, operation in severe environments, lightness, compactness, and high reliability will force a strong trend toward modular construction, and particularly toward microelectronics and other new high-density complex components." The report goes on to predict that such components will be used in 40 percent of the military electronic equipment for receiving functions procured in 1970.

To provide for you the Navy's insight into this sort of prediction, we are fortunate to have with us today a top expert on what the Navy's requirements are as reflected in the field of microelectronics. Admiral Roeder has been involved in communication work for most of his entire Naval career. His first assignment in this field was in 1937 when he was ordered to duty in the Communications Division of the Office of Chief of Naval Operations.

During the World War II he served as communications officer on various staffs, including some arduous sea duty. He received the Legion of Merit for service in World War II. During the Korean conflict he was Commander of Destroyer Division 12, participating in much of the heavy action including the siege of Wonsan.

For these actions he was awarded two gold stars in lieu of second and third Legions of Merit. In 1957 he was able to plunge himself again into his area of technical interest, communications, when he was appointed Deputy Director for Naval Communications in CNO. Finally, in June 1960, he was assigned his present post as Assistant Chief of Naval Operations for Communications and Director of Naval Communications.

Admiral Roeder brings a dedicated and enthusiastic interest to this post. He is greatly concerned with the electronics systems which are needed to solve the increasingly challenging problems that our Navy faces today. I think you will find him a man with dynamic ideas of his own but intent also on learning the ideas of others.

May I present our keynote speaker who will highlight the performance ideals of the Navy in this field - Rear Admiral Bernard F. Roeder.

MICROELECTRONICS FOR THE NAVY – PROMISE OF AN IDEAL

Rear Admiral Bernard F. Roeder, USN
Assistant Chief of Naval Operations (Communications)
Director, Naval Communications

According to one computer expert, there are several hundred computers in this room. He is said to have described the human body as a ten-cycle computer in a one-tenth of a ton chassis with a one-tenth of one horsepower motor.

The most marvelous example of microminiaturization – inclusive of a measurable amount of electrical energy, is said to have been with man for hundreds of thousands of years, if not millions.

Thus far man has been unable to equal the seemingly inexhaustible capabilities of his own brain with any instrument or combination of instruments he has yet devised. But he is working on the challenge.

Man's brain may be said to be microelectronics' best endorsement. What appropriations committee is going to go against it?

Size and weight reductions, without loss of desired capabilities, have been sought since the known beginnings of Navies. However, to say that the Navy is interested in the promise of reductions in size and weight from microelectronics is to overly simplify the Navy's interest; it does not give recognition to many other promises from a new technology which are at least as important to us.

World War II electronics – compounded by postwar electronics developments – revolutionized United States Naval Communications in the aggregate. During these years certain new capabilities appeared that met new needs, new operational requirements. They were imposed by world tensions which continue, the outbreak and threatened

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This, the keynote address of the Conference, was presented on the second day when some 375 representatives from industry joined some 135 government electronics and materials experts in listening to the papers presented during the second and third days of the Conference.

outbreak of limited wars, and this country's new responsibilities. In this climate, the United States Navy was and is required to go to sea with oversize, overweight and overly complex systems of black boxes that have bled the Navy white in technical personnel.

The Navy had no choice, then, and has none now. However, the glimmer of the promise of an alternative is appearing on the horizon. This is the first time during the long and awkward age of modern electronics that the Navy has been given hope. There will be no regrets from us when we can refer to the era of the big, black box in past tense.

What lies beyond the revolutionary changes expected to be brought about by the promise of microelectronics is difficult to envision at this point, except further miniaturization. When present difficulties with materials are resolved, as they will be, systems and circuitry takeover by microelectronics appears to be the key to the future.

The big, bad black box has been the most expensive necessity ever laid on a Navy. The appetite of this outsized, short lived, fragile beast is voracious and insatiable. For example, sprawling and prone, it consumes valued shipboard space; consumes logistics support; demands too many attendants and keepers to make it as well behaved as it is; is responsible for more down time than up; during its short life it is estimated to cost its owners from four to ten times its initial cost. Overall it has taken a huge bite out of the operational Navy. In short, the beast is on report with a list of charges as long as your arm, yet the Navy has had to live with it in crowded spaces.

Only necessity and the lack of feasible, superior alternatives have justified continuation of the existing situation without relief.

Through this era, successive Directors of Naval Communications have repeatedly addressed themselves to industry, seeking its solution to the size, weight, complexity and logistics problems attendant to modern electronics and the black box in the operational Navy.

With the advent of a miniaturized electronics technology we are not going to start arguing against features we have been seeking for years. For the operational Navy, microelectronics seem to hold the promise of an ideal. This ideal is inexorably leading the Navy toward microelectronic systems and toward the prospect of vast evolutionary changes years from fulfillment. The hope and the prospects of rescue have come none too soon.

What may microelectronics give us that we do not have? Do we want it? If we want it, how much do we want? And how do we get there?

If the Navy said today that it wanted to microelectronic all electronic systems in a modern destroyer, how long would it take a combination of Navy and industry to get there, starting now with the present state of the art and the electronic industry's present capability?

One interested group cites the following potential advantages promised by microelectronics -

Size and weight reduction.

Increased reliability.

Reduced maintenance.

Reduced cost.

Reduced lead time.

Better power utilization. And -

Increased equipment capabilities per unit weight and per unit volume.

Another list enumerates as potentialities savings in space, weight, power and cost, increases in reliability and improved maintainability, while permitting development of new devices and functions that are not possible with conventional electronic components.

Concurring in the foregoing, I should like to add the following -

The advantages of production line techniques and the prospects of sharply declining costs under rising production.

Rapid operational restoration.

Sharp reductions in the requirements for technically trained personnel aboard ship.

Increases in the speed of electronic circuits.

Smaller, faster and more maneuverable ships.

More fully operational ships and aircraft through sharp reductions in down time.

Doubling or tripling firepower in smaller ships without doubling or tripling costs.

Better utilization of shipboard spaces.

Reductions in crews.

The prospect of superior resistance to salt spray and humidity.

The requirement for less power. This reduction in power equates to the requirement for less space for the ship's generating equipment.

Reductions in radiated power equate to less heat, offering the prospect of smaller air conditioning systems or their elimination, and the release of spaces they now occupy.

The potential of equating the survivability of microelectronic equipment to the survivability of the ship itself -- now very unequal.

The prospect of superior "Radiation Resistance."

Reduction or elimination of duplicate functions by automating functions now performed by personnel with greater error, slower speeds and low reliability.

What does microelectronics promise to give us that we do not have? The prospect is, just about everything that we do not have but want.

How do we get there?

There are at least three basic approaches. Avionics already is the point of entry for one of them. That is, taking certain pieces of systems and duplicating those pieces which are interchangeable mechanically and electrically with discreet circuitry, with which the existing system is built.

Another approach is to take a system instead of a piece and proceed similarly with the system as was done with the piece.

A third approach is to break with the past, get away from the ancient paths of conventional circuitry and take advantage of the promises of the new technology. This involves taking a look at the entire system, starting out at the beginning of the program and locking in the new early, and locking out the old.

There is no doubt that we stand at an historic juncture for the third time in most of our lifetimes. The first was at the introduction of radio itself; the second was at the advent of electronics, and the third is the threshold of microelectronics.

It is understandable that different points of view should prevail at this juncture, and they do. This is healthy. It is competitive. Doubtless there is merit in all the new technologies, in degree, as well as some demerit, in degree, technique against technique.

There is intellectual agreement on the advantages of standardization, but there is disagreement on the standards. Standardization for the military is necessary and it is inevitable. Therefore, who can and should referee the issue of standardization toward early resolution?

Misuse, misinterpretation and misunderstanding of terms in the new technology, and the loose use of its language, can be costly to user and supplier. Early and continuing agreement on definitions is mandatory that all principals may talk a common language and that contractual verbiage may be divested of ambiguities present otherwise. The promise of this new technology will be even brighter for the military user if early and continuing resolution of the language barrier in this growing technology is made by the electronics industry. A start in this direction is not enough.

Admittedly, certain technologies are in contention. In the early days of radio many techniques were in contention also. Much is being discussed and argued without proof. A prototype Navy ship may be the referee and testing platform to assist in pointing up performance differences of new techniques under operating conditions. De Forest sailed part way with the great White Fleet of President Theodore Roosevelt. De Forest, the Navy and industry learned much of value from this. Marconi was employed to send the Navy's first official wireless message. The shipboard techniques employed were his and were in his hands. Radio was the revolutionary instrument to great changes and greater capabilities that microelectronic technology also promises.

One mothballed ship could be selected as the experimental vehicle, the ship's systems undergoing conversion to total microelectronics, one system employing one of the new techniques and another system a second, and so on, from fire control, surveillance and ship control to communications.

It has been said by some in the electronics industry that they are "talking the problem to death without deciding anything."

A microelectronicized destroyer, leaving electromechanical devices and high power vacuum tubes intact, could tell a great deal that we do not know and do so with comparative economy in relationship to what we would learn about the actual maintainability, shock resistance, reliability, life, radiation resistance, speed, heat radiation, and so on, of microelectronics and about the comparative merits of the competitive technologies, using the sea as the proving ground and the ship as the vehicle. A great deal of guessing would be eliminated.

How far can microelectronics go? Well, how small is small?

It no longer is "How small" or "How light." There are other qualifiers. For example, the relative weightlessness of superminiaturization may be attractive to avionics until the superficial attractiveness vanishes at the sight of dollar costs for initial purchase, replacements, attending personnel which microelectronics presumably reduced, and the hazards of exotic microelectronics techniques in operation. Each size reduction may utilize different techniques with each technique propounding new evaluation factors. Microminiaturization in electronics can possibly go further than the Navy may desire to go in the foreseeable future.

Microelectronics is almost certain to change the shape of ships as electronics now is doing. At present the Navy is building an aircraft around a microelectronics package. The future may see surface ships similarly built around packaged microelectronics systems, with integrated control in a single master control room.

Microelectronics can learn from the dark past of the black box. For years electronics equipments and systems were added where there was space on and in the ship, and sometimes added when there wasn't. It was almost the game of pin the tail on the donkey - blindfold. The shape of many new ships reflects the recognition of the necessary marriage between ship and electronics. The age of microelectronics may see capsulated ships built around capsulated electronics.

Now is the time to hear from users. Let us not wait until after development of a device to speculate on the user's application, whether ashore, submerged, airborne or at sea.

What better immediate targets for microelectronics than known prospective users in the military, known operating environments with daily experiences in discreet systems and black boxes? Concentration of effort on knowns is usually more productive and less wasteful than diffusion of effort on unknowns.

Whereas microelectronics may revolutionize electronics and the electronics industry, microelectronic systems for the Navy may be anticipated to be on the order of evo-revolutionary.

The end of the vacuum tube may or may not be in sight. Whether it is or is not, microelectronics offers the Navy family the first promise of retiring the black box to the Smithsonian Institution as a gargantuan electronics object for future generations to behold.

The possibility and the time of fulfilling this promise are in your hands.

Introduction to Contractors' Report Session

Captain S. F. Balaban, USN
Office of Naval Research
Washington, D.C.

Good Morning Gentlemen:

Before I introduce the scheduled speakers, I would like to add a footnote to Admiral Roeder's keynote address. I am sure that his expressed concern about the black-box problem is accepted by all of you as a challenge--a really big job for little microelectronics.

I would venture further to say that as a conference the acceptance of this challenge might be divided into three groups along the following lines: First, those of you who are working hard on current electronics projects will go back to your jobs and struggle with old circuit or specification problems. To you, the future marvels of microelectronics are not much help and your prime concern is to deliver to the customer another black box. Your work is important to the Navy, and we want the best you can produce--but unfortunately your finished product will only add to our growing inventory of black boxes and contribute adversely to the overwhelming maintenance problem Admiral Roeder mentioned. To you, micro is not much help today and perhaps you have got your fingers crossed about it being the Utopian solution of the future.

The second group, among you, may be made up of marketing people and Vice Presidents. Your acceptance of this challenge is vastly different from the first group. Perhaps you have already whispered to your neighbot--"If that's all the Navy wants, we've got it on the shelf." or "We have done it for NASA in project so and so- or that's old stuff to us, we're delivering to Minuteman that kind of reliability." Well, it is indeed fortunate that this group is here today because the speakers are going to talk about some real problems before production can start in microelectronics.

Now, the last group--which I think constitutes the majority of you, accepts this challenge with a full understanding that there is a big pay-off over the horizon--but much hard work lies ahead to solve the problems of this explosive new electronics technology. Yes, problems with passive as well as active elements--problems with interconnections as well as component isolation, etc.

I would like to associate all the Navy people here today with this group. We want to joint you in solving today's problems so that we can in the not too distant future realize the wonderful potentials associated with microelectronics. We are reasonably familiar with the tough technical problems but we are convinced that with your help they can be solved--and when this happens, the Navy may have for the first time its long sought objective of high reliability and performance in electronics.

PROGRESS IN THIN FILM COMPONENTS

H. W. Katz
General Electric Company
Syracuse, New York

I. Introduction

The major objective of the program which was recently completed by the General Electric Electronics Laboratory for NADC[1] involved the development of linear circuits in microelectronic form. The specific circuit functions were to be chosen from the "Handbook of Selected Semiconductor Circuits," NObsr 73231. The circuits would perform the same electrical functions in terms of the input-output terminals, although the choice of internal components would be dependent on the prevailing microelectronic techniques. Considerable effort had already taken place in the development of digital microelectronic circuits, since the available techniques were most readily adaptable to digital systems rather than linear circuitry. Hence, this program was an attempt to partially fill a missing portion of the circuit spectrum.

The circuit design problems which are created by the various microelectronic approaches are in large part due to the limited types of components, as well as the range of available parameters. In conventional design and packaging techniques the utilization of separate transistors, diodes, resistors, capacitors, and inductors, permits almost unlimited combinations of design techniques to optimize the circuits for particular applications. The severest restriction at the present time in any of the microelectronic approaches is, of course, the lack of suitable inductors. An inductor essentially stores a certain amount of magnetic energy per unit volume. Hence, if the available volume is considerably restricted, the total inductance can only be achieved by considerable increases in the numbers of turns or the utilization of extremely high closed gap permeable cores. The number of turns which can be deposited by today's techniques is, of course, quite limited, and the development of high permeability materials deposited in situ has lead to extremely small inductor values with relatively poor Q factors. The relatively high d.c. resistance of the deposited wires partially accounts for the Q.

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[1] Contract N62269-1335. The major contributors to this program were Dr. V. Russell, Dr. D. Stockman, Dr. J. Blank, Dr. A. Cahill, G. Danielson, and J. Lawler.

Hence, linear microelectronic circuits would have to be redesigned with only resistors, capacitors, and transistors. For the present program, low frequency circuits were chosen since this presented a greater challenge to both the circuit designer and the fabricator of microelectronic circuits, due to the need for capacitors of relatively high capacitance per unit area. The circuits which were ultimately chosen were an audio oscillator, an audio amplifier, and a tuned amplifier. However, the major problems existed in the development of suitable capacitors.

II. Capacitor Development

The attainment of large capacitors is, of course, dependent upon the proper combination of high dielectric constant material and very thin dielectrics. The simplest approach is simply to deposit an extremely thin dielectric layer onto a previously deposited conductor. However, there are reasonably severe limitations to this procedure. If the dielectric thicknesses ranged in the order of 100 Å, the device would no longer function as a capacitor, since other conductive mechanisms, such as tunneling or field emission would take place. Furthermore, such small film thickness may lead to pinhole problems. Hence, attention was directed toward the utilization of higher dielectric constant materials at thickness ranges of a few thousand Å.

This paper will discuss the results obtained by three different approaches. The first consisted of the utilization of anodized tantalum capacitors which were deposited in multiple layers, the development of the glow discharge technique for the deposition of mixed oxides, and finally the anodization of evaporated aluminum.

A. Stacked Tantalum Capacitors

Figure 1 illustrates the configuration which could yield reasonably large capacitors. The objective was to deposit alternate layers of tantalum and tantalum oxide, and thus develop an array of parallel capacitors. Each of the tantalum layers was deposited by a sputtering technique. The glass plate was then removed from the sputtering apparatus and used as one electrode in an anodizing bath in which the opposite electrode was a tantalum sheet and the solution was ethylene glycol. The anodizing voltage was normally in the range of 20-50 volts with almost complete anodization taking place within five minutes. However, successive depositions of sputtered tantalum created a condition in the oxide film which usually led to shorted capacitors. Furthermore, the d.c. anodization technique yielded capacitors which exhibited an unsymmetrical electrical characteristic. Considerably improved oxide layers were obtained when an a.c. (60 cps) voltage was applied during the anodization process rather than a d.c. voltage. This process produced capacitors with symmetrical characteristics. If four such capacitors were stacked together, it was possible to achieve approximately four microfarads per square inch with a dissipation factor of about six per cent and a breakdown voltage of approximately 3-4 volts. This process was reasonably useful for capacitors deposited over an area of $\frac{1}{2}$" x $\frac{1}{2}$".

The technique, however, was not further developed, since a reasonably large number of processing steps were required which necessitated the removal of the glass plate from the sputtering apparatus into the anodizing bath for each capacitor. This would not lend itself to satisfactory process control nor simple fabrication technology.

B. Glow Discharge Techniques

Those materials which exhibit the highest dielectric constant comprise the class of titanates, such as barium or lead titanate. The dielectric constant of such materials ranges from the order of 100-1000. Thus, for reasonable thicknesses, one could achieve capacitors in the order of fifty microfarads per square inch. However, the usual technique for processing such materials consists of mixing together the oxides of the various constituents in powder form and then pressing them together with a binder, and subsequently firing the mix at relatively high temperatures. This technique is obviously incompatible with the usual thin film technology. However, it is possible to achieve the same compounds by a glow discharge process. The apparatus for this procedure is illustrated in Figure 2. Volatile organic compounds which contain metal ions that are required for the final film are introduced into the bell jar, together with oxygen. The high voltage initiates a discharge or ionization of the oxygen gas, as well as the organo-metallic compound. The metal ions then react with the oxygen on the substrate to form the desired compound.

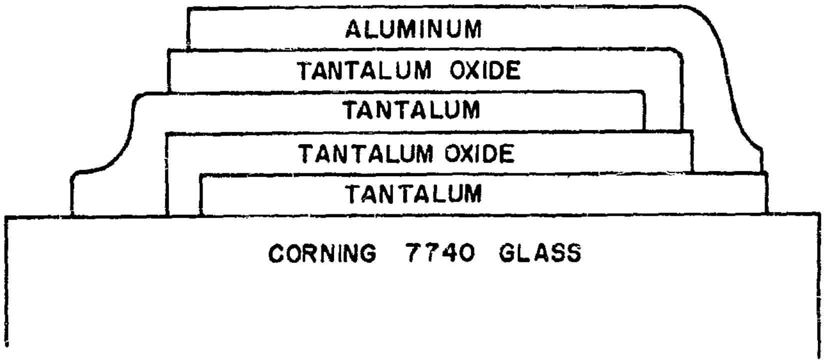

ALUMINUM
TANTALUM OXIDE
TANTALUM
TANTALUM OXIDE
TANTALUM
CORNING 7740 GLASS

Figure 1 - Schematic Diagram of a Stack of Tantalum Oxide Capacitors

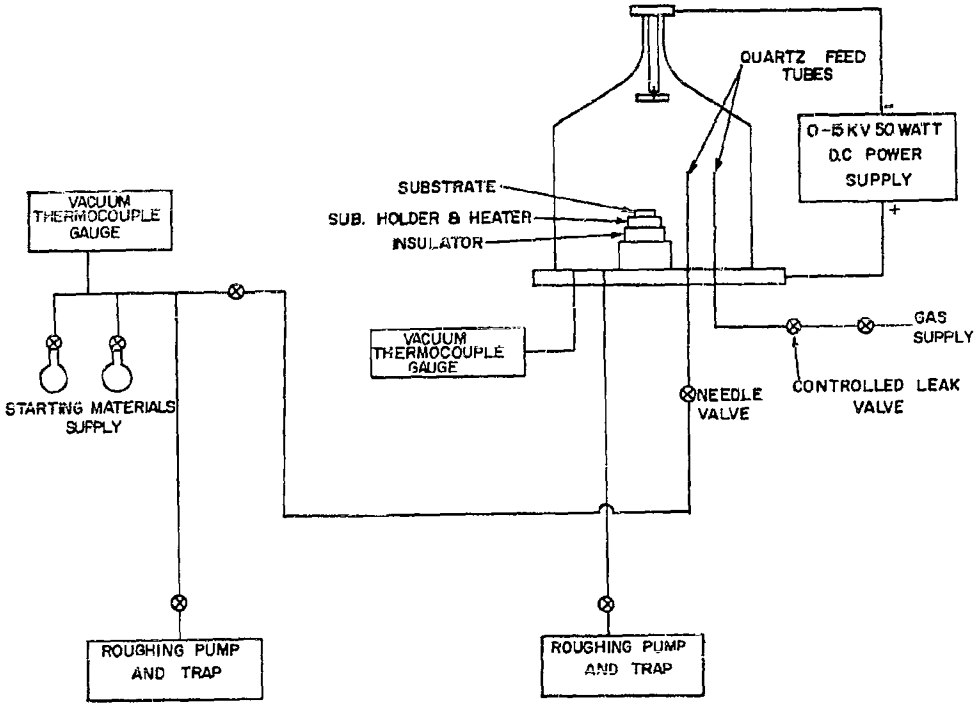

QUARTZ FEED TUBES
0-5 KV 50 WATT D.C POWER SUPPLY
-
+
SUBSTRATE
SUB. HOLDER & HEATER
INSULATOR
VACUUM THERMOCOUPLE GAUGE
VACUUM THERMOCOUPLE GAUGE
STARTING MATERIALS SUPPLY
GAS SUPPLY
NEEDLE VALVE
CONTROLLED LEAK VALVE
ROUGHING PUMP AND TRAP
ROUGHING PUMP AND TRAP

Figure 2 - Schematic Diagram of Gloe Discharge Apparatus

This process was first tried for a simple oxide, such as TiO_2. In this case the organic compound was titanium tetraisopropylate. TiO_2 was deposited onto gold electrodes, which were previously placed on a glass slide. The resultant films as analyzed by X-ray diffraction were shown to be amorphous. Subsequent infrared analysis showed that no organic matter was present. At thickness ranges of approximately 5,000 Å, it was possible to achieve one microfarad per square inch with a dissipation factor of less than 3%. However, the frequency response indicated about a 1% change in capacitance between 1 kc and 100 kc.

Since the process was evidently under good control, it would have been desirable to try the deposition of barium titanate. However, it was not possible to obtain a sufficiently volatile organic compound which contained barium. Hence, it was decided to try lead titanate for which suitable materials are available. In this case titanium tetraisopropylate was introduced into the glow discharge apparatus in addition to tetra-ethyl lead. Although the volatility of these two compounds are approximately the same, a one-to-one starting ratio did not result in a one-to-one ratio of lead to titanium in the deposited film. Since the dielectric constant of this material is a strong function of ratio of lead to titanium, the highest dielectric constants could not be achieved. Furthermore, initial success with this material were difficult to reproduce. The source of this difficulty was later traced to variations in the purity of the original constituents. As it turned out, the manufacturer had removed small traces of isopropylate alcohol from the titanium tetraisopropylate. Small additions of this particular alcohol improved the volatility characteristics, such that suitable films could be deposited. Although this technique was not continued, it still offers one of the best possibilities for achieving the deposition of mixed oxides for unusually large capacitor values.

C. Anodized Aluminum

The most successful capacitors which we have developed to date have been the anodized aluminum. Although anodized bulk aluminum usually does not yield very good capacitors, due probably to the lack of uniformity of the aluminum, and particularly the inclusion of impurities such as carbon; it was considered highly desirable to try this process for evaporated aluminum for two reasons. One, the interconnections on the glass substrate are usually made with evaporated aluminum; and hence, one electrode of the capacitor would be deposited at the same time as the conductors. Secondly, the evaporated aluminum could be considerably freer of impurities, and hence, lend itself to successful anodization.

These capacitors were formed by anodizing the aluminum in an ethylene glycol solution provided with a suitable wetting agent. At an anodizing voltage of 20-50 volts and film thickness of less than Å, it was possible to achieve approximately two microfarads per square inch with dissipation factor less than 1% and breakdown voltages in the order of 20 volts.

III. Circuit Configurations

As indicated above, the major problem in the circuit design was to rearrange the configuration so that the same functions could be performed as outlined in the standard circuits handbook, utilizing only RC and transistors. In addition, component values and the number of components were to be chosen so that the entire circuit could be deposited on a single glass base.

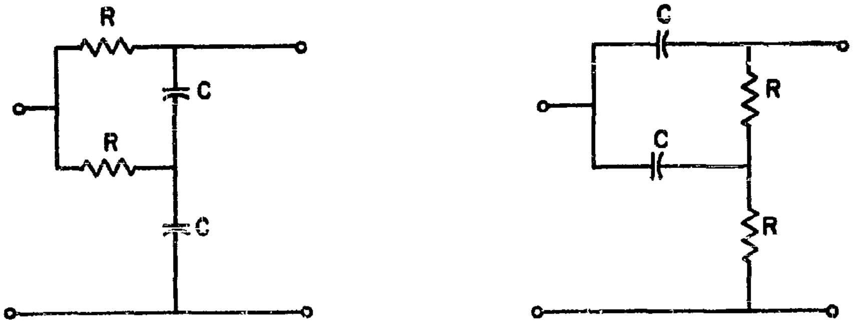
A. Low Frequency Oscillator

In the oscillator design it is necessary to obtain a circuit which will have the required closed loop phase shift and an open loop gain of greater than one, in order to maintain the oscillating state. Furthermore, it was very desirable to have a circuit which could also eliminate coupling capacitor as well as the by-pass capacitors to simplify the overall construction.

The criterion for obtaining a gain greater than one was realized through the use of two RC networks shown in Figure 3. These networks have the property that over a specified frequency range, the voltage transformation ratio is greater than one, as shown in Figures 4 and 5. The networks use the same values for the resistors and capacitors. However, one of the networks uses a lagging phase shift, while the other produces a leading phase shift. In combination with two transistors which essentially isolate the networks from each other but provide no voltage gain, it is possible to construct a relatively efficient oscillator, which meets the above conditions. This oscillator is shown in Figure 6. The frequency of the oscillator, assuming no loading by the transistors, is given by

$$f = \frac{1}{2\pi RC}$$

The two additional RC filters were added in the output section to reduce the harmonic distortion. In this particular circuit the values of capacitors are sufficiently low so that silicon monoxide was used as the dielectric, which considerably simplified the fabrication.



LAGGING PHASE RC NETWORK

LEADING PHASE RC NETWORK

RC PHASE SHIFT NETWORKS

Figure 3

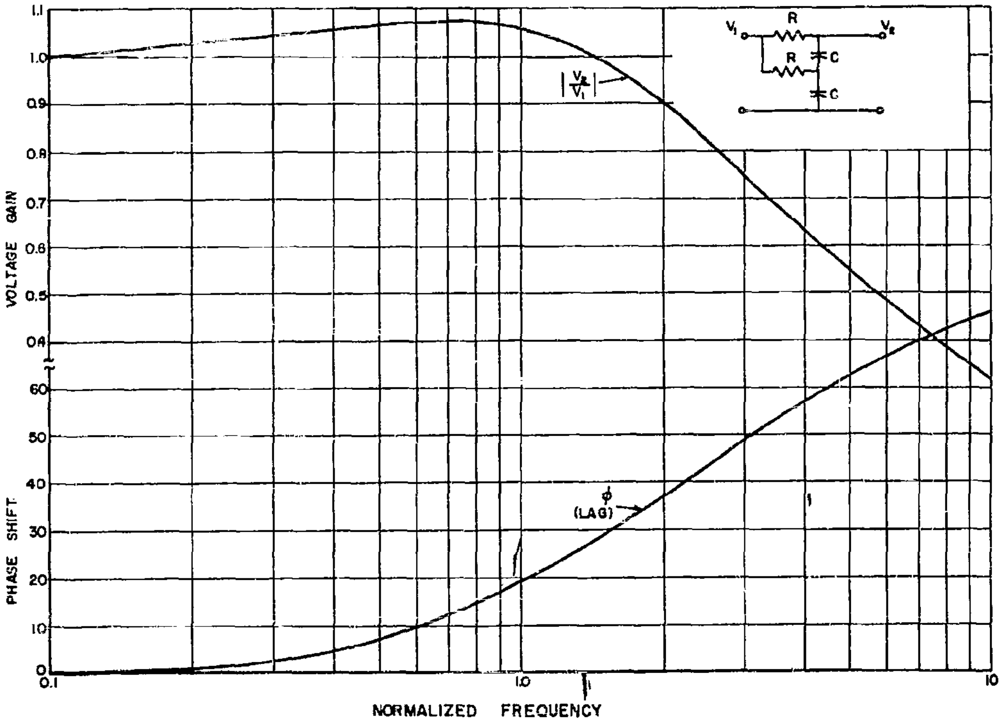


Figure 4

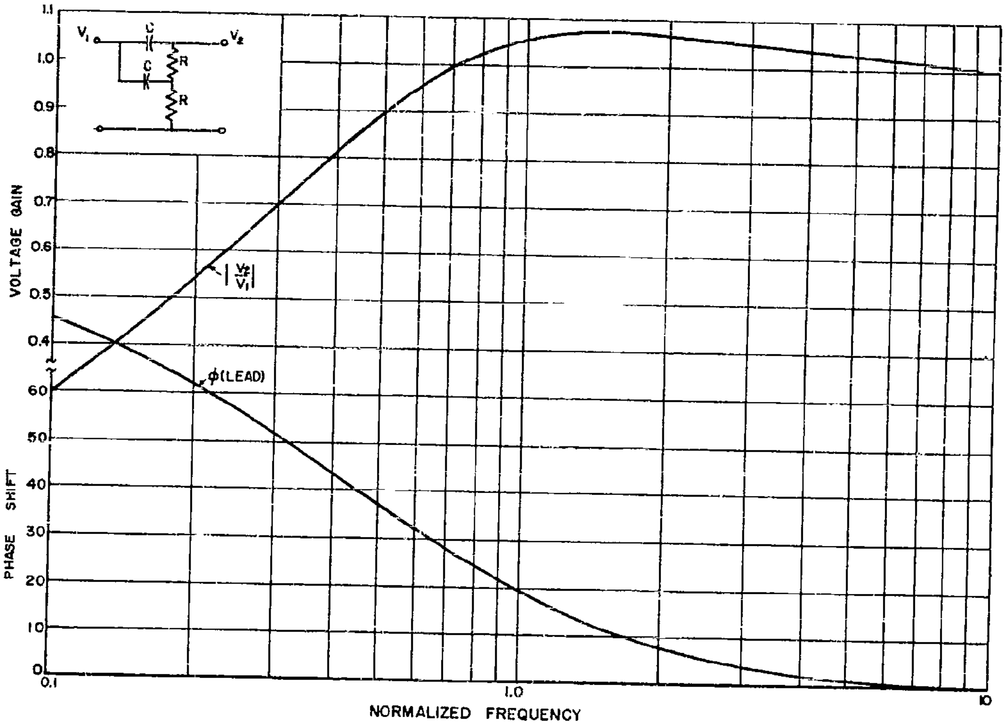


Figure 5

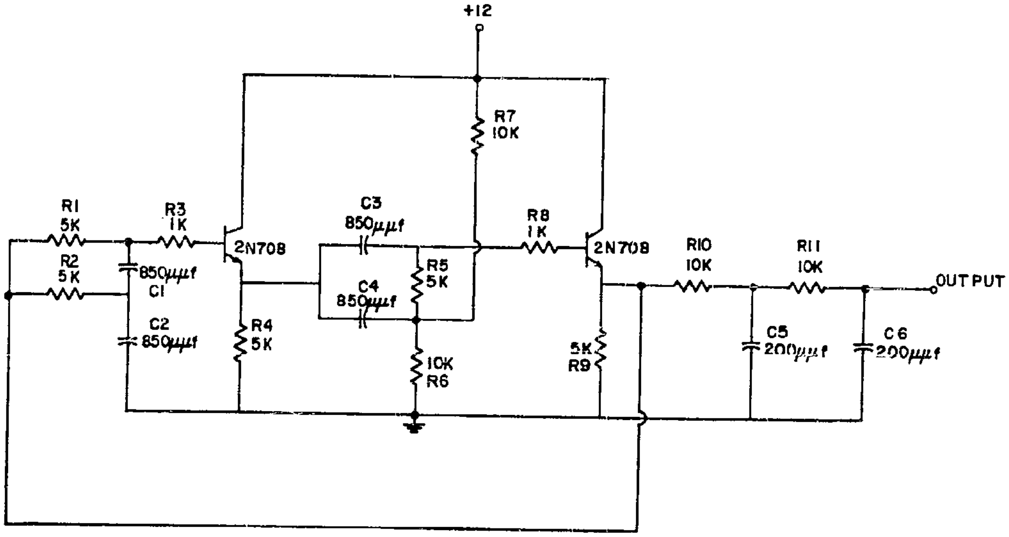

+12
R7
10K
R1
5K
R2
5K
R3
1K
850μμf
C1
C2
850μμf
2N708
R4
5K
C3
850μμf
C4
850μμf
R5
5K
10K
R6
R8
1K
2N708
5K
R9
R10
10K
R11
10K
C5
200μμf
C6
200μμf
OUTPUT

Figure 6 - RC Oscillator

Six such oscillators similar in function to circuit 5-11 of the "Handbook of Selected Semiconductor Circuits" were fabricated, whose operating frequencies were within 10% of the design value of 37.5 kc. The oscillators were also tested over the temperature range, 0° C. to 40° C. The shift in frequency was approximately 500 ppm/$^\circ$C. This total drift consists of temperature variations of the resistors and capacitors which are approximately 80 ppm/$^\circ$C. and 200 ppm/$^\circ$C. respectively. The remainder of the variation is probably due to the temperature dependent loading of the transistors which results from the variation of β with temperature.

The variations of frequency due to supply voltage changes were approximately .15% volt.

B. Tuned Amplifiers

The tuned amplifier selected for fabrication has a center frequency of 455 kc, a bandwidth of 20 kc and a voltage gain of about 60 db and operates from sources of plus 12 volts and minus 12 volts. The tuned amplifier schematic is shown in Figure 7. It is functionally similar to circuit 4-7 in the "Handbook of Selected Semiconductor Circuits." The selectivity is achieved in a two stage RC feedback amplifier, which is buffered at its input and output with an added stage. The amplifier center frequency is given very closely by

$$f_o = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

and Q is given by

$$Q = \frac{\text{center frequency}}{\text{bandwidth}}$$

$$= \frac{\sqrt{R_1 C_1 R_2 C_2}}{R_1 C_1 + R_2 C_2 - R_2 C_1}$$

Since the desired amplifier response cannot be obtained without very close control over the tolerances on R_1, R_2, C_1 and C_2, the resistors R_1 and R_2 were fabricated with several tap positions. The amplifier can then be aligned before potting by selecting the proper combination of taps.

The frequency response of the amplifier is shown in Figure 8.

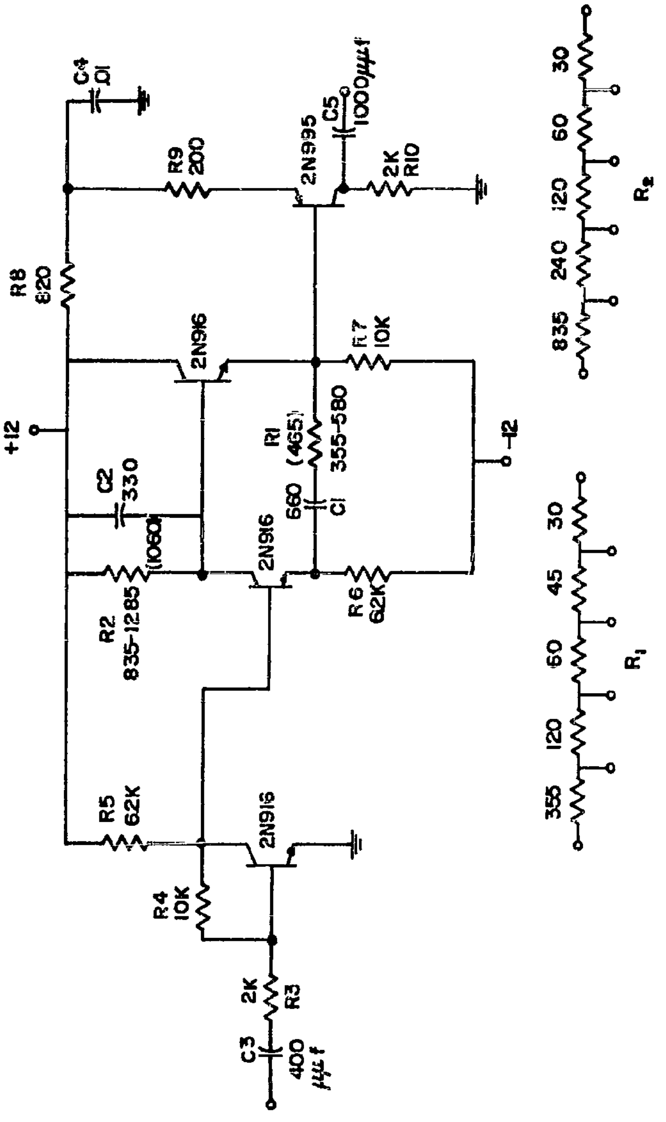

C4
.01
R9
200
2N995
C5
1000μμf
2K
R10
R8
820
2N916
R7
10K
+12
C2
330
R1
(465)
355-580
-12
560
C1
(1060)
2N916
R2
835-1285
R6
62K
R5
62K
2N916
R4
10K
2K
R3
C3
400
μμf
835
240
120
60
30
R2
355
120
60
45
30
R1

Figure 7 - Tuned Amplifier

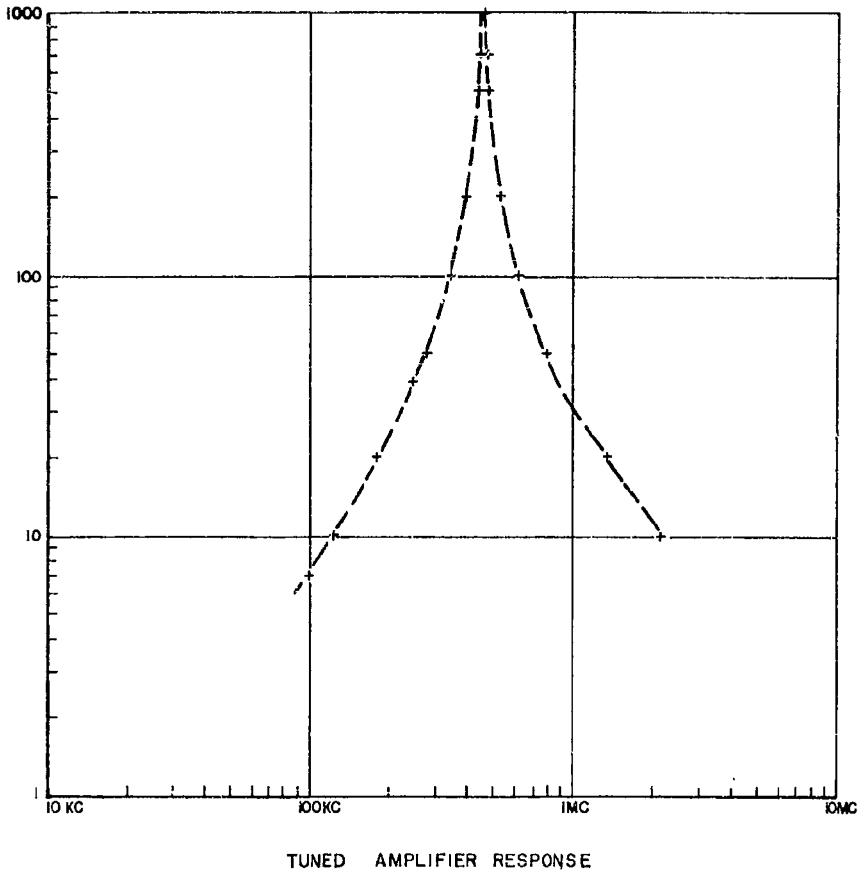
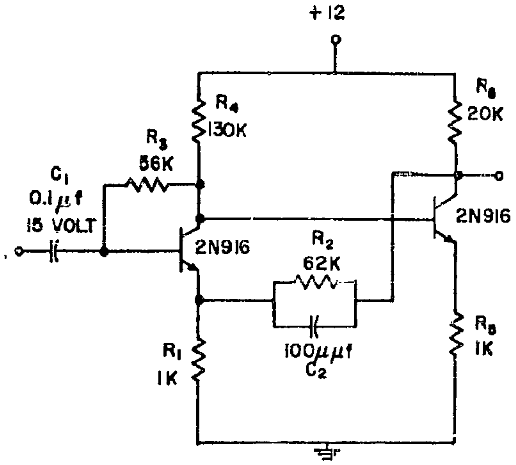


Figure 8 - Tuned Amplifier Response

Figure 9 - Audio Amplifier


+12
R4
130K
R3
56K
C1
0.1μf
15 VOLT
2N916
R2
62K
100μμf
C2
R1
1K
R6
20K
2N916
R5
1K

C. Audio Amplifiers

The audio amplifier selected for fabrication was a two stage feedback amplifier providing a voltage gain of about 55 over the frequency range of 120 cps to 25 kc, and operates from a single 12 volt source at a current level of about 0.5 ma. The audio amplifier is shown schematically in Figure 9, which is functionally similar to circuit 3-7 in the "Handbook of Selected Semiconductor Circuits." The amplifier voltage gain is approximately determined by the resistor ratio R_2/R_1 (the actual voltage gain is about 10% lower than this). Series feedback is employed at the input in order to raise the input impedance level and thus extend the low frequency response. However, the biasing resistor R_3 reduces the input impedance to about 14 KΩ and produces a low frequency roll-off at about 120 cps. This bias scheme is simple and not critical. Variation in V_{BE} with temperature for the two transistors tend to cancel. Variations in β with temperature result in a variation of the voltage across R_3, but this drift can be tolerated at the output. The capacitor C_2 was added to produce a high frequency roll-off at 25 kc.

The audio amplifier characteristics are shown in Figure 10.

The amplifiers were tested over a temperature range from -40° C to +40° C. in which the voltage gain variations remained ± 0.6 db. The drift in output bias voltage with temperature is tabulated in Table IX.

IV. Circuit Fabrication

The thin film circuits described above were deposited on 0.6" by 0.6" Pyrex slides. The slides were cleaned in the conventional manner by an ultrasonic process followed by vapor de-greasing. The first deposition consisted of the nickel-chromium resistors which were evaporated through a mask. A 10 mil width and a one to two minute deposition time yields resistances between 200 and 500 ohms per square inch. The substrate is heated to approximately 300° C. during deposition.

At a second station within the vacuum system the aluminum conductor pattern is then evaporated through a second mask. The circuits had been designed to eliminate crossovers to simplify some of the fabrication. A layer of silicon monoxide was then evaporated over the resistors as a protective coating and also as a capacitor material in the case of the oscillator circuit. The counter electrodes were evaporated as the final deposition. In those cases in which a larger capacitor was required, the plates were removed from the vacuum system and the aluminum electrodes were anodized. Packaged micro-miniature transistors were then attached to the films by thermo-compression bonds. The leads to the circuit were .013" diameter gold wire. The completed circuits were embedded in epoxy resin and packaged in accordance with NADC specifications.

V. Conclusion

The development of these low frequency linear circuits indicates the versatility of thin film techniques in meeting the various requirements of circuit design. However, further component development is still required in order to further improve the range of RC parameters and their stability under extended environmental conditions. Furthermore, techniques should be sought which would improve the compatibility between thin films and all-semiconductor networks.

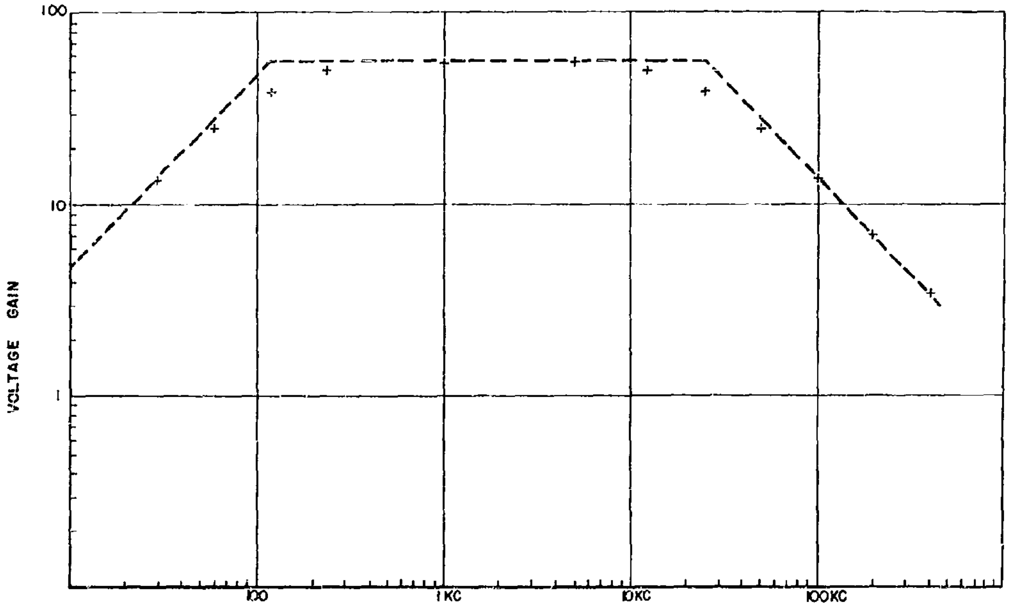


Figure 10

THE PREFERRED MICROELECTRONIC FUNCTION PROGRAM

L. H. Stember, Jr., Director
Advanced Electronics Group
Battelle Memorial Institute
Columbus, Ohio

INTRODUCTION

This paper briefly describes Battelle's program for the Naval Air Development Center entitled "Preferred Microelectronic Functions" (Contract No. N62269-1717). The program will be presented as follows: (1) the objectives, (2) the research team, (3) the approach, and (4) what the microelectronics (μE) industry can do to assist the Navy in this effort.

OBJECTIVES

The objectives of this project are the following:

(1) Investigate methods of characterizing μE functions

(2) Develop functional descriptions for selected high-usage functions

(3) Make recommendations for R & D in μE techniques.

The intent of the program is to make the functional descriptions as general and as flexible as possible while retaining the desirable qualities of performance standards. This should allow the functions to be implemented by many different microelectronic (μE) techniques, yet give the Navy and system designers the advantages of readily available basic building blocks.

THE RESEARCH TEAM

The research team has been selected from three groups in Battelle's Engineering Physics Department as shown in Table 1. This provides the program with backgrounds in μE, reliability, circuit analysis, circuit design, and semiconductor and thin-film techniques.

TABLE 1. THE RESEARCH TEAM

Battelle Institute	Project
ENGINEERING PHYSICS DEPARTMENT	Preferred μE Functions
ADVANCED ELECTRONICS GROUP [μE and Reliability]	Over-all Project Direction and Team Member (EE)
ELECTRICAL ENGINEERING GROUP [Design]	Team Member (EE)
ELECTRONIC MATERIALS AND DEVICES GROUP [Semiconductor and Thin-Film Techniques]	Team Member (Physicist)

THE APPROACH

The program is outlined in Figure 1. There are two primary phases of the program which are concurrent. One is the investigation and development of methods to characterize and specify the performance of electronic functions, and the other is the selection of high-usage circuits that are amenable to microminiaturization to use as examples for characterizing functions.

Investigation and Development of Methods

Many methods of specifying electronic functions are being considered. Transfer characteristics are obvious means of describing these functions. These characteristics can be plotted as a graph versus a critical parameter such as temperature or frequency with tolerance limits to specify satisfactory performance. Function

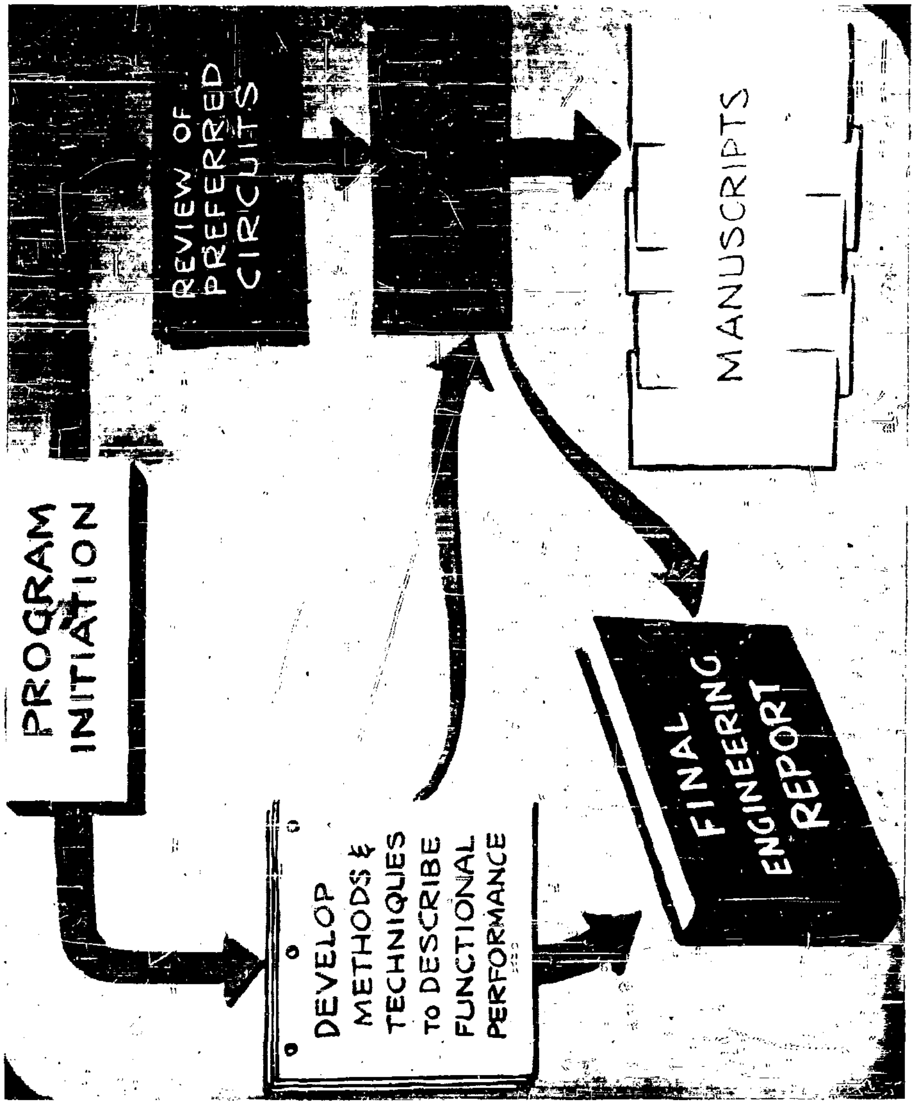

PROGRAM INITIATION
DEVELOP METHODS & TECHNIQUES TO DESCRIBE FUNCTIONAL PERFORMANCE
REVIEW OF PREFERRED CIRCUITS
MANUSCRIPTS
FINAL ENGINEERING REPORT

FIGURE 1. GENERAL PROGRAM OUTLINE

parameters may also be presented in tabular form with maximum, typical, and minimum values. Stress limits may also be included in the tables.

Another type of functional description planned to be used is the performance profile, which is sometimes known as a schmoo plot or a marginal checking curve. These are graphs that show the interactions between critical functional parameters of the microcircuit. They may be used to let the systems engineer know how close to its limits he is pushing the circuit and what design margins he is allowing. These may also be used in the design and fabrication of microcircuits. For the latter purposes, they define criteria which the circuit must meet in spite of production tolerances or drift.

The profile of Figure 2 shows a microfunction with an input voltage E_{IN}, a d-c energy source E_B, and an output voltage E_O. The output voltage E_O has a failure criterion which states that it must be greater than y and less than x. The curves on the graph encompass the area that represents the combination of E_{IN}, and E_B values which will permit E_O to remain within the failure criterion. As the input voltage is decreased, a point is reached where the output signal is too low to meet the requirements. Also as the input signal is held constant and the energy source is decreased, the circuit again does not meet the requirements ($E_O > y$). The failure criterion (that E_O must be less than x) is exceeded as the energy source voltage is increased or as the input voltage is increased. The square around the nominal point on the graph indicates what system conditions the microcircuit will see in a typical system. A measure of the design margin is the distance between this nominal area and the failure curves. It is evident that the design margin is wide in this instance.

Circuit Review Analysis and Research and Development Report

The concurrent phase of the program is described in Figure 3. It may be seen that, as these various methods are being investigated and developed, they are being tried on specific circuits. A screening process was used to select specific circuits for examples. This step was based on Navy's Preferred Circuit Program. The functions described by these preferred circuits were reviewed and compared to the functions used in a selected group of Navy airborne systems. The functions were thus rated in order of their usage. The preferred circuit functions were also evaluated from a standpoint of amenability to microminiaturization based on state-of-the-art restraints such as power, voltage, parameter tolerances, need for adjustable parameters, etc. Then from these listings of high-usage and high-amenability, the circuits which will be used as guinea pigs for the characterization were selected. After detailed

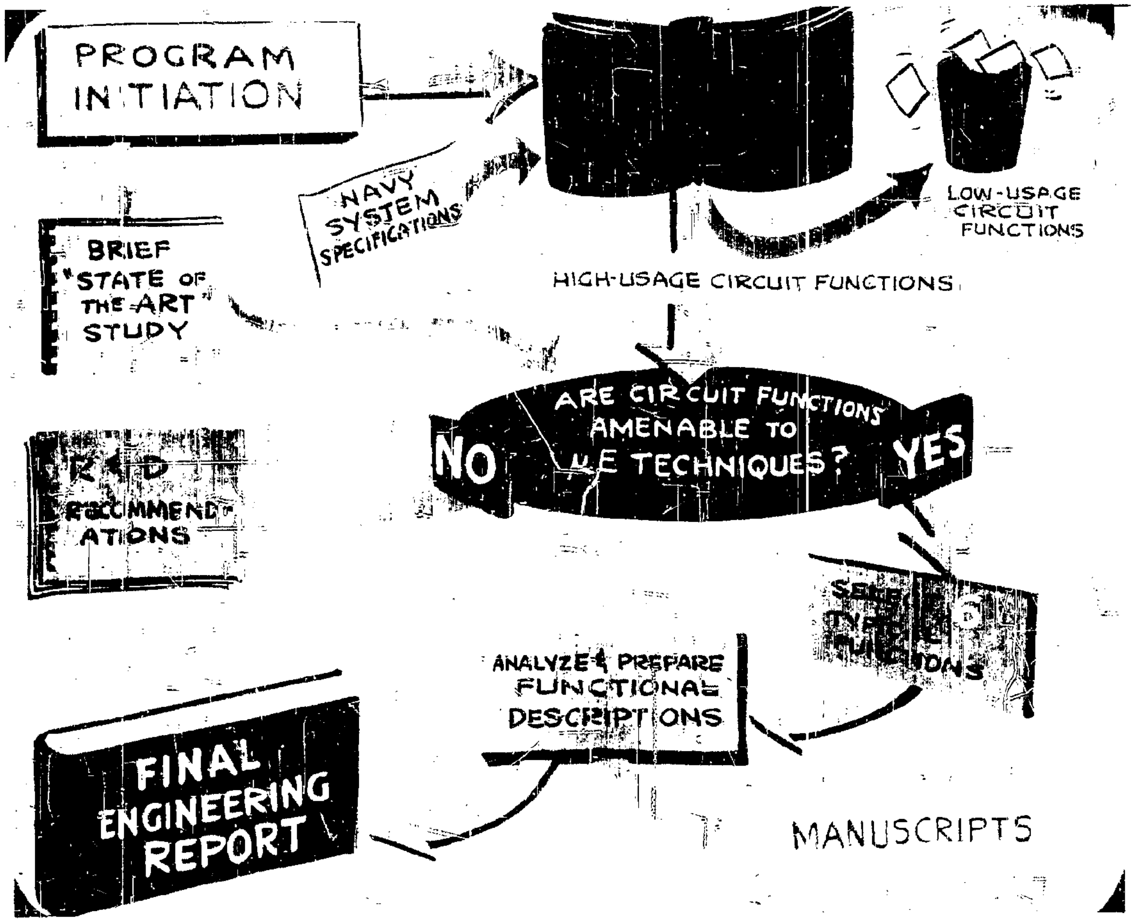

PROGRAM INITIATION
NAVY SYSTEM SPECIFICATIONS
LOW-USAGE CIRCUIT FUNCTIONS
HIGH-USAGE CIRCUIT FUNCTIONS
BRIEF "STATE OF THE ART" STUDY
ARE CIRCUIT FUNCTIONS AMENABLE TO μE TECHNIQUES?
NO
YES
R & D RECOMMEND-ATIONS
ANALYZE & PREPARE FUNCTIONAL DESCRIPTIONS
FINAL ENGINEERING REPORT
MANUSCRIPTS

FIGURE 3. OUTLINE OF CIRCUIT REVIEW AND ANALYSIS PORTIONS OF PROGRAM

analysis and laboratory studies are made on these circuits, functional performance descriptions will be prepared. These manuscripts will form a basis for the preparation of item requirement sheets for Specification EL5-13A, "General Specification for Microelectronic Modular Assemblies".

The information obtained from this review, together with knowledge of the state of the art, provides the background against which a set of R & D recommendations is being written. These recommendations will be made on the basis of circuits that are not directly amenable to microminiaturization. They will be directed toward basic and applied research that should permit the reliable microminiaturization of more high-usage circuits.

HOW YOU CAN ASSIST

This discussion should leave you with a thumbnail sketch of the project. I would certainly be happy to receive written descriptions of your companies' current microelectronic design philosophies to make these functional descriptions as current as is feasible. The main goals of these descriptions are to generally specify functions as functions without tieing them down to a specific circuit schematic to allow many different techniques to be used in implementing these functions. This should enable systems designers to have reliable, easily obtainable, economical hardware available for their use. Any suggestions or reports that you feel would contribute to this program can be sent to the address listed below:

L. H. Stember, Jr., Director
Advanced Electronics Group
Battelle Institute
505 King Avenue
Columbus 1, Ohio

Requests for reports resulting from the project should be directed to:

Howard Martin, Head
Electronic Technology Laboratory
Development Support Division, AEEL
Naval Air Development Center
Johnsville, Pennsylvania

A FILM ELECTRONICS AIRBORNE COMPUTER

W. N. Carroll
International Business Machines Corporation
Kingston, New York

INTRODUCTION

The use of thin-film techniques to reduce the size and weight of military airborne electronics has generated considerable interest throughout the industry during the past few years. Extensive research and development programs are currently being pursued by numerous companies, both within the United States, and, abroad, to refine the vacuum deposition process to be used for the fabrication of thin-film equipment. One of the earliest applications of thin-film techniques to airborne equipment is being made by IBM at its Kingston, New York Laboratories. This equipment is being designed to perform the computing function of a weapon-delivery system.[1]

This particular application was chosen for the thin-film electronics computer since the required functions are well defined and could be readily converted into digital form, and because the limited complexity of the system will permit an early appraisal of thin-film techniques at a minimum cost.

The various ballistic equations which had to be solved by the system were carefully analyzed in order to determine the required computer organization. As a result of this analysis, it was determined that a fixed-point, stored-program, general-purpose digital computer would meet the desired system accuracy.

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[1] The work reported on in this paper is being done under contract to the Naval Avionics Facility, Indianapolis, Indiana, and is scheduled for delivery by the middle of 1963. Many of the techniques and processes described have been developed under previous contracts with the Naval Avionics Facility and the U. S. Army Signal Research and Development Laboratories, Ft. Monmouth, New Jersey.

The basic block diagram of the thin-film computer is shown in Figure 1. The system includes, in addition to the general purpose digital computer, a 11-channel analog-to-digital converter, a 7-channel, manual input section, and a 5-channel output section. A self-contained, 3-phase, 400-cycle power supply will also be provided.

Some of the salient features of the general purpose digital computer are listed in Table 1.

Table 1

- General Purpose Synchronous
- Parallel Operation
- 26-Bit Data Word
- 13-Bit Memory Word
- 1024 Memory Words
- Fixed Program
- 16 Instructions
- 500-KC Clock Rate
- 80°C Maximum Ambient Operating Temperature

CIRCUIT DESIGN

The first packaging level of this computer consists of integrated thin-film circuit panels. These panels include the passive components of 32 circuits and various intercircuit connections. Between 70 and 80 of these panels will be required for the computer.

The first step in the design of an integrated film panel is the selection of a basic circuit. The choice of this circuit is governed by the system requirements, as well as the present state-of-the-art of film fabrication. The selected circuit must be readily fabricated in a film format, and should posses logic design flexibility. The present state of film component reproducibility excludes the integral deposition of critical components with tolerances smaller than ± 5 percent. In addition, the number of power supplies required should be minimized to simplify the power distribution on the integrated film circuit panel. Fabrication costs can be reduced and the reliability improved by minimizing the number of non-deposited components, such as transistors, diodes, and inductors. In addition, micro-miniature packaging densities necessitate a circuit power dissipation in the low milliwatt range.

To satisfy all these requirements, transistor-resistor logic (TRL) employing the NOT-OR (NOR) function was chosen as the basic circuit of the integrated thin-film panel. The circuit speeds (2 mc) achievable with TRL meets the requirements of the system design. The specific circuit selected is shown in Figure 2. A 2N744 silicon epitaxial transistor was used in the circuit design. Table 2 lists the circuit design specifications.

Table 2

Item	Specification
Transistor Type	2N744
Beta min	40
Veb min	0.58 V
Veb max	0.85 V
Vec min	0.10 V
Vec max	0.25 V
Fan in	3
Fan out	3
Power Supply Voltage	+6V
Supply Tolerance	±4%
R in	4000 ohms
R out	1000 ohms
R Tolerance	±4%
Power Dissipation Max.	61.83 mw
Power Dissipation Typical	40 mw
Minimum Lower Level Voltage	0.1 V
Maximum Lower Level Voltage	0.25 V
Minimum Upper Level Voltage	2.9 V
Maximum Upper Level Voltage	5.3 V
Maximum Frequency	2 mc
Typical Delay	50 nsec.

CIRCUIT TOPOLOGICAL LAYOUT

An integral part of the design is the topological layout of the film circuits. Such considerations as optimum component placement, power distribution, and in-process monitoring of the passive components must be included in the overall circuit design. Two topological layouts for the basic circuit are shown in Figure 3. The one on the left represents an earlier layout which employed 250 ohms-per-square cermet resistors, and placed two circuits in a 0.310 by 0.435 inch area. With this ohms-per-square value, the 1000-ohm output resistor was defined by a 46.5 mil by 185 mil rectangle; the 4000-ohm input resistors by a 15 mil by 240 mil rectangle. The layout on the right represents the latest design and will be used in the fabrication of the computer. This layout, although electrically identical to the older version, incorporates several important improvements. Resistors are deposited at 1000 ohms per square, resulting in a significant increase in component density. A smaller, hermetically-sealed 2N744 transistor has been obtained from a commercial vendor which is compatible with both the new layout and the solder attachment process already developed. The circuit layout uses a minimum resistor width of 25 mils, which substantially reduces the effect of mask tolerances upon the electrical parameters of the circuit. In addition, the circuit incorporates jumper patterns which allow the alternate use of the basic topological layout as an emitter follower driver. Such a driver is capable of driving up to 25 basic circuits in parallel, a necessary feature for the design of the computer. The overall area required by this new layout is 0.250 by 0.350 inch.

The land areas and conductors of the circuit are formed by depositing copper over a chromium underlay through appropriate masks. Silicon monoxide is used for insulation and dielectrics.

The resistor material used in both layouts is a chromium-silicon monoxide mixture (cermet) which is flash-evaporated by a powder-feed source. To obtain 250 ohms-per-square values, a ratio of 70 percent chromium to 30 percent silicon monoxide is used. For 1000 ohms-per-square values, the mixture is changed to approximately 40 - 60, the exact ratio being dependent upon the film thickness and deposition temperature. These cermet resistors which are deposited through masks on a silicon monoxide underlayer have shown exceptional stability and uniformity under severe environmental conditions. Tabel 3 categorizes the environmental tests conducted on representative samples of these resistors.

Table 3

Ohms-per-square range	250-4500
Fabrication tolerance	± 5%
Resistor range	1-30,000
Temperature Coefficient	-25 ppm/°C

Table 3 (continued)

Stress Condition	ohms/sq.	Samples	Storage Time	% R	Power Range
200°C Storage	250	100	2000 hrs.	.2%	None
200°C Storage	4500	20	1000 hrs.	.6%	None
300°C Storage	250	50	2000 hrs.	.3%	None
300°C Storage	4500	20	1000 hrs.	.3%	None
High Humidity at 60°C	250	20	1000 hrs.	1.2%	0-1.5w/in^2
Power Test at 25°C	250	50	5000 hrs.	.2%	10-20w/in^2
150 Cycles of Temperature Humidity Power Test (Mil-Std-202-Method 106A)	250	50	3500 hrs.	3%	0-11w/in^2

NOTE: All of the above samples had no environmental protection except an SiO overcoat.

PANEL LAYOUTS

In the design of the panels, such factors as the desired circuit interconnection densities, component-packing densities, size and cost of a throw-away package, shock and vibration requirements, and the maximum area permitting the required fabrication control, have to be considered.

Figure 4 shows an early design which contained 56 TRL NOR circuits on a 2.5 by 3.5 inch substrate. This particular assembly, a four-stage binary counter with controls, provides for all necessary intercircuit connections in the horizontal and vertical channels between the circuits. The 44 output tabs at the bottom of the panel are designed to be attached to specially-designed pin connectors. All transistors on the panel are simultaneously attached by a solder reflow process. Assemblies produced by this method have successfully withstood 600-G shock and 2000-cycle vibration with 50 G's loading. The output waveforms of this panel, shown in Figure 5, are equal to or improved over those obtained with conventional NOR circuits. To change the particular logic function contained on the panel, only the interconnection paths need be changed. Figure 6 is the logic of one bit of a parallel arithmetic element; it is being fabricated for a small feasibility model, and is an example of the logic complexity which can be placed on such a panel.

Completely assembled panels (Figure 7) include a frame for mechanical support, and a pin connector for connection to the back panel. The back panel is comprised of a multilaminated printed circuit board to which the female portion of the connector is dip soldered.

Large panel sizes, such as needed for the 56-circuits, require the lamination of two panels back to back about an epoxy interlayer to meet shock and vibration requirements, resulting in a throw-away unit containing 112 circuits. To minimize throw-away costs, a smaller substrate (2.5 by 2 inches,) containing 30 circuits with the same topological layout, was fabricated. This panel (Figure 8) does not require the double-panel sandwich to meet shock and vibration requirements due to its smaller area.

A second problem area is the variety of interconnection patterns required . Although films were used for the circuit interconnections, and sufficient paths were available to provide the desired functions, the technique of deposition through masks necessitated many different mask types to accommodate the various patterns. To eliminate this difficulty, a new method of obtaining the interconnection patterns has been developed by combining chemical-etching techniques with vacuum deposition and masking.

This approach permits a design which enables all interconnection variations to be obtained from a single vacuum deposition sequence. The required patterns are obtained by etching an initial copper deposition, and depositing a standard jumper and insulation pattern. Figure 9 shows the basic principal of this technique. After depositing an undercoat of silicon monoxide over the entire substrate, a chrome-copper coating is deposited and chemically-etched to produce most of the interconnection pattern. In areas of the panel allocated to cross-overs, a standard silicon-monoxide insulation pattern is deposited to provide the necessary insulation. A jumper pattern is then deposited through a standard mask to complete the connections. With this process, masking for the integrated film panels is identical regardless of the particular functional layout. Variations in the inter-circuit connections are obtained by etching techniques.

The panels which will be used to fabricate this first thin-film computer will incorporate these improvements. Figure 10 shows the improved integrated film panel layout, which contains 32 circuits on a 1.865 by 2.5-inch substrate, and incorporates the universal interconnection pattern. All panels for the logic sections of the computer will be identical with regard to the evaporation process.

MEMORY DESIGN

The memory required by the system contains 1000 13-bit words, and consists of 14 panels of 32 by 32 ferrite cores. These cores have a 19-mil inside diameter and a 30-mil outside diameter, and are contained in a volume of 2-1/4 by 1-1/4 by 3/4 inches. Drive and sense circuitry for this array will be fabricated with film components on the standard 1.865 by 2.5 inch substrates, and will be contained on 12 panels. The memory array, which is pluggable, is used for both the non-destructive, fixed operational program and the read-write temporary storage requirements of the computer. The fixed operational program is permanently wired into the array. The core material being used for this memory has demonstrated satisfactory performance over temperatures from -30°C to +120°C.

INPUTS AND OUTPUTS

Manual inputs and discrete outputs are handled by standard digital techniques. For the analog-to-digital conversion, a technique involving a series of approximations is being considered. Figure 11 shows the block diagram for the proposed converter. To maintain the desired accuracy, a 11-position converter is required. Most of the circuitry for this converter can be handled by the standard logic panels. Special film panels will be designed for those applications which can not be handled by the basic circuits. Where needed, precision components in either bulk or film form will be attached in the manner used for the active elements. It is estimated that the analog-to-digital converter can be packaged on approximately 10 panels.

POWER

The prime power for the computer is obtained from the 400-cycle, 3-phase power on board the aircraft. This power is transformed into the main computer supply of +6V, and into two special voltages: +15V for the memory current drivers, and +10V ±0.1 percent, for the analog-to-digital converters. The power supply, as well as the entire computer, is immersed in a liquid for cooling and environmental protection. The anticipated volume for the power supply is 50 cubic inches.

OVERALL PACKAGING

Figure 12 shows the computer as presently planned. Eighty to 100 film panels of approximately 20 types, a ferrite memory core array, the analog-to-digital converter, and the power supply will be placed in an assembly having dimensions of 9 by 9.25 by 3 inches. Total estimated weight is approximately 20 lbs. Each film panel is provided with a special connector to provide easy maintenance. A single, multilayered back panel is used for all inter-panel connections, and special connectors are placed on the top of the assembly for input-output signals. Total power consumption for the computer is approximately 150 watts; it is estimated that the hot-spot temperature can be kept below 105°C, in an ambient temperature of 80°C.

TABLE 4. COMPUTER SIZE AND WEIGHT ESTIMATES

MAJOR ITEM	UNIT PARTS	NUMBER OF PANELS**	PANEL TYPES	VOLUME (cu. in.)	WEIGHT (lbs.)
Central Computer		68	18	68	3.8
	Instruction Register and Command Generator	5			
	Address Register	3			
	Oscillator, Timing Ring	3			
	Arithmetic Control	3			
	Arithmetic Section	40			
	Program Counter	3			
	Memory Address Register	8			
	Output Buffers	3			
Memory		18	4	21	1.5
	Drive and Sense Circuits	12			
	Diode Memory	6			
	Memory Core Array *			2.11	
Analog-to-Digital Converter		10		15	1.0
	Multiplexer	2			
	Control Logic	4			
	Amplifier Compare Circuits	4			
Power Supply				50	5.0
Mechanical Housing and Liquid Coolant				75.25	5.8
Miscellaneous Hardware and Back Panel				20.5	1.0
Total Computer				249.75	18.1

* Memory Array = 2 1/4" x 1 1/4" x 3/4" inches.

** Each panel is approximately 1 cubic in. in volume, and weighs .055 lbs.

ACKNOWLEDGEMENT

The author acknowledges the contributions made to this work by his many associates at the IBM Engineering Laboratory in Kingston, New York, in particular, to Mr. J. W. Skerritt, Dr. R. E. Thun, and Dr. A. E. Lessor for their valuable contributions to the project, and to the preparation of the paper.

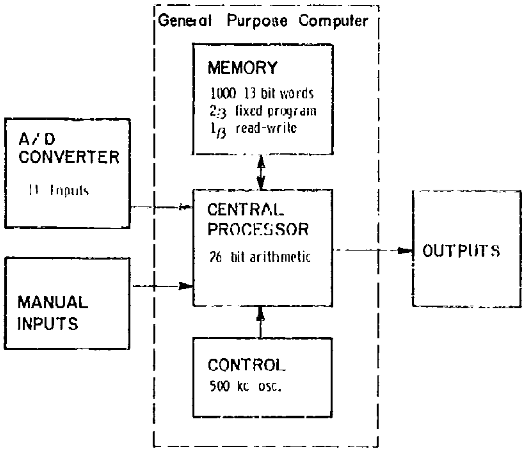
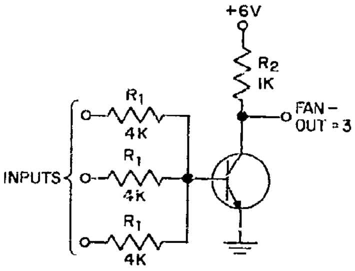
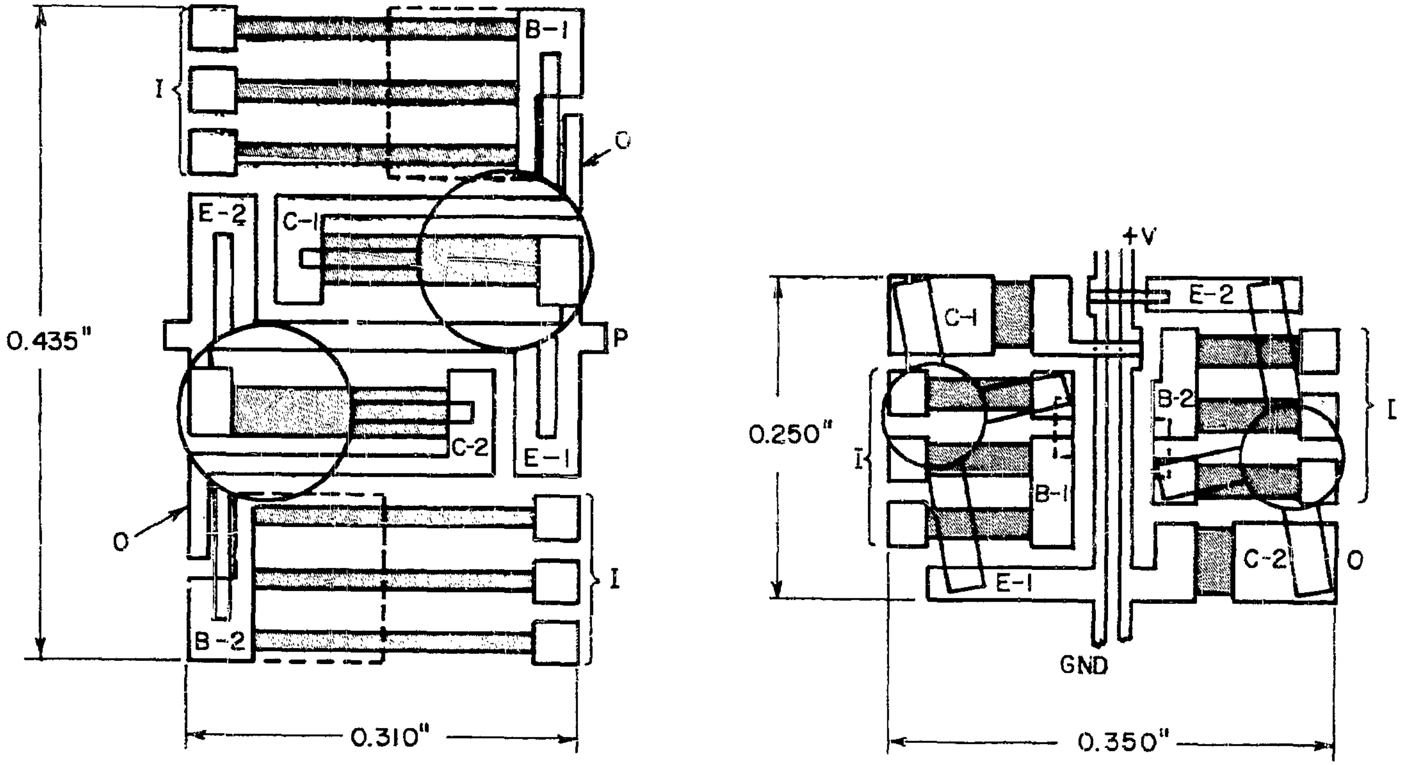

General Purpose Computer
MEMORY
1000 13 bit words
2/3 fixed program
1/3 read-write
A/D CONVERTER
11 Inputs
CENTRAL PROCESSOR
26 bit arithmetic
OUTPUTS
MANUAL INPUTS
CONTROL
500 kc osc.

Figure 1 - Film Electronics Computer (Block Diagram)

Figure 2 - TRL-NOR Basic Circuit


+6V
R2
1K
FAN-OUT = 3
R1
4K
R1
4K
R1
4K
INPUTS


I
B-1
O
E-2
C-1
0.435"
P
C-2
E-1
O
I
B-2
0.310"
+V
E-2
C-1
0.250"
I
B-2
I
B-1
C-2
O
E-1
GND
0.350"

RESISTORS — 250 Ω/□

RESISTORS — 1000 Ω/□

Figure 3. Topological Layouts Of A TRL-NOR Basic Circuit

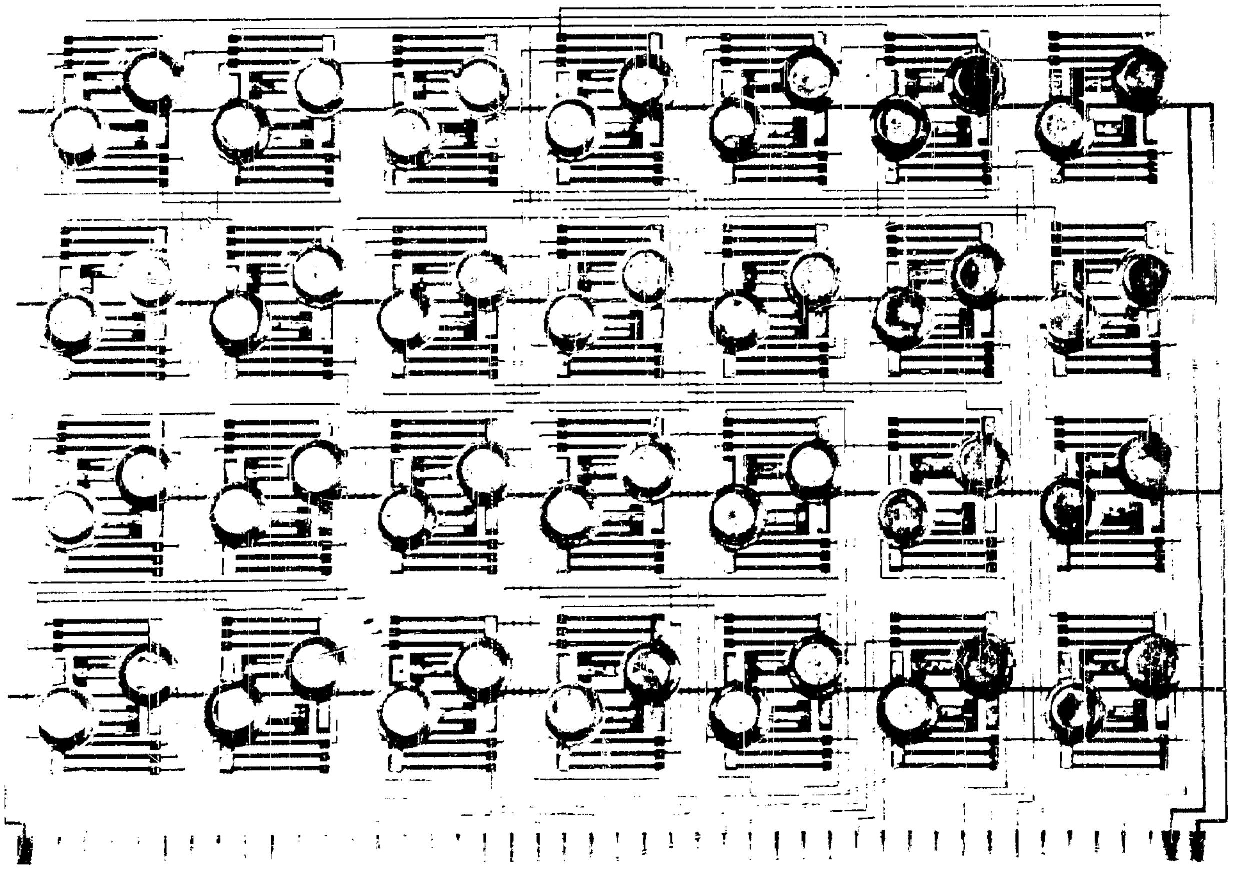


Figure 4 - Integrated Film Panel

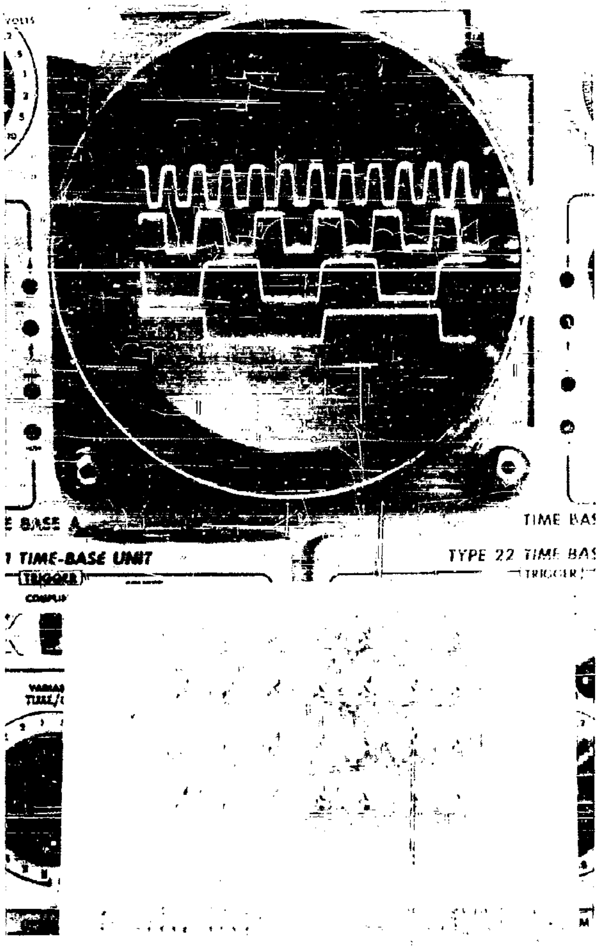

VOLTS
E BASE A
1 TIME-BASE UNIT
TRIGGER
TIME BAS
TYPE 22 TIME BAS
TRIGGER

Figure 5. Integrated Counter Assembly Operating at 2.5 mc

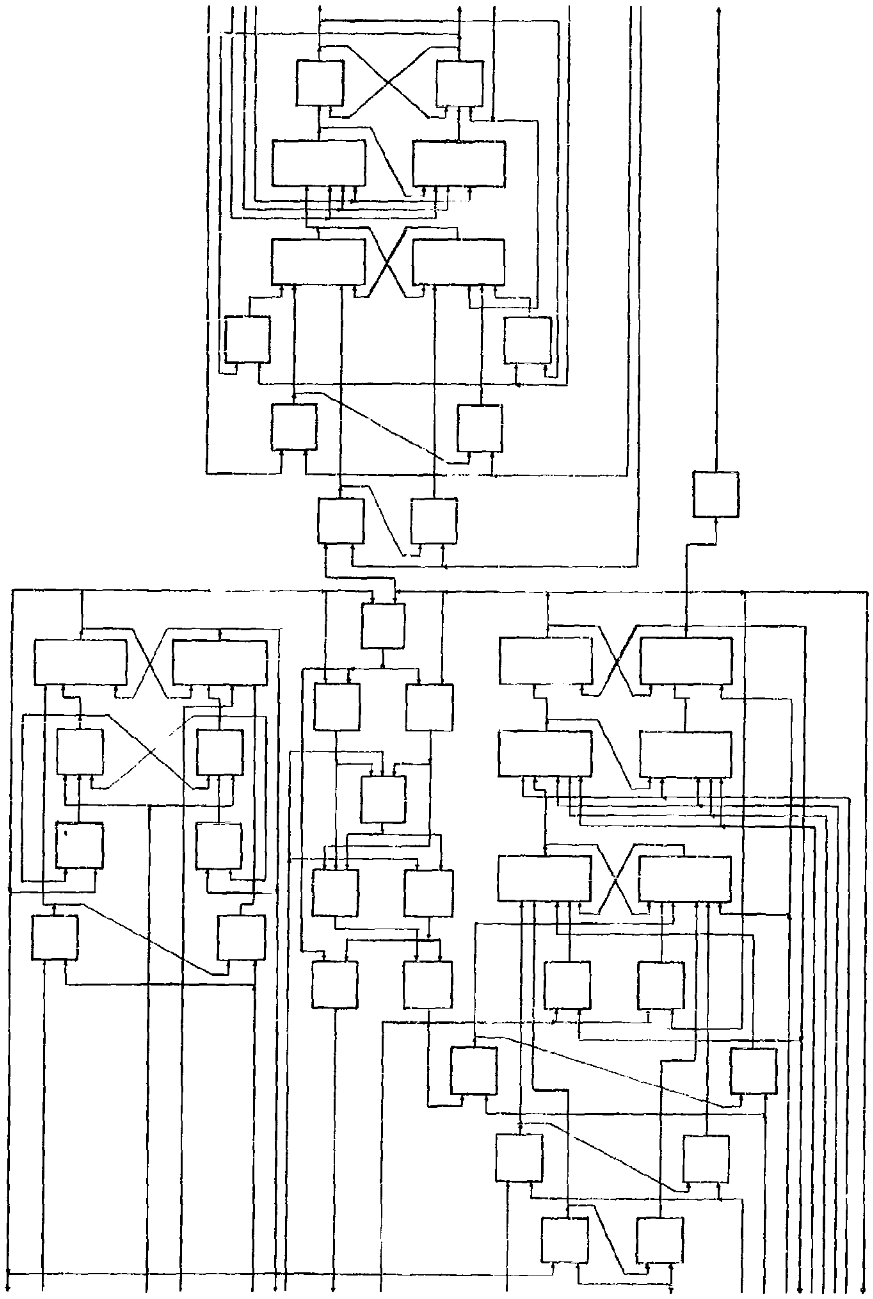


Figure 6. Logic for Arithmetic Panel

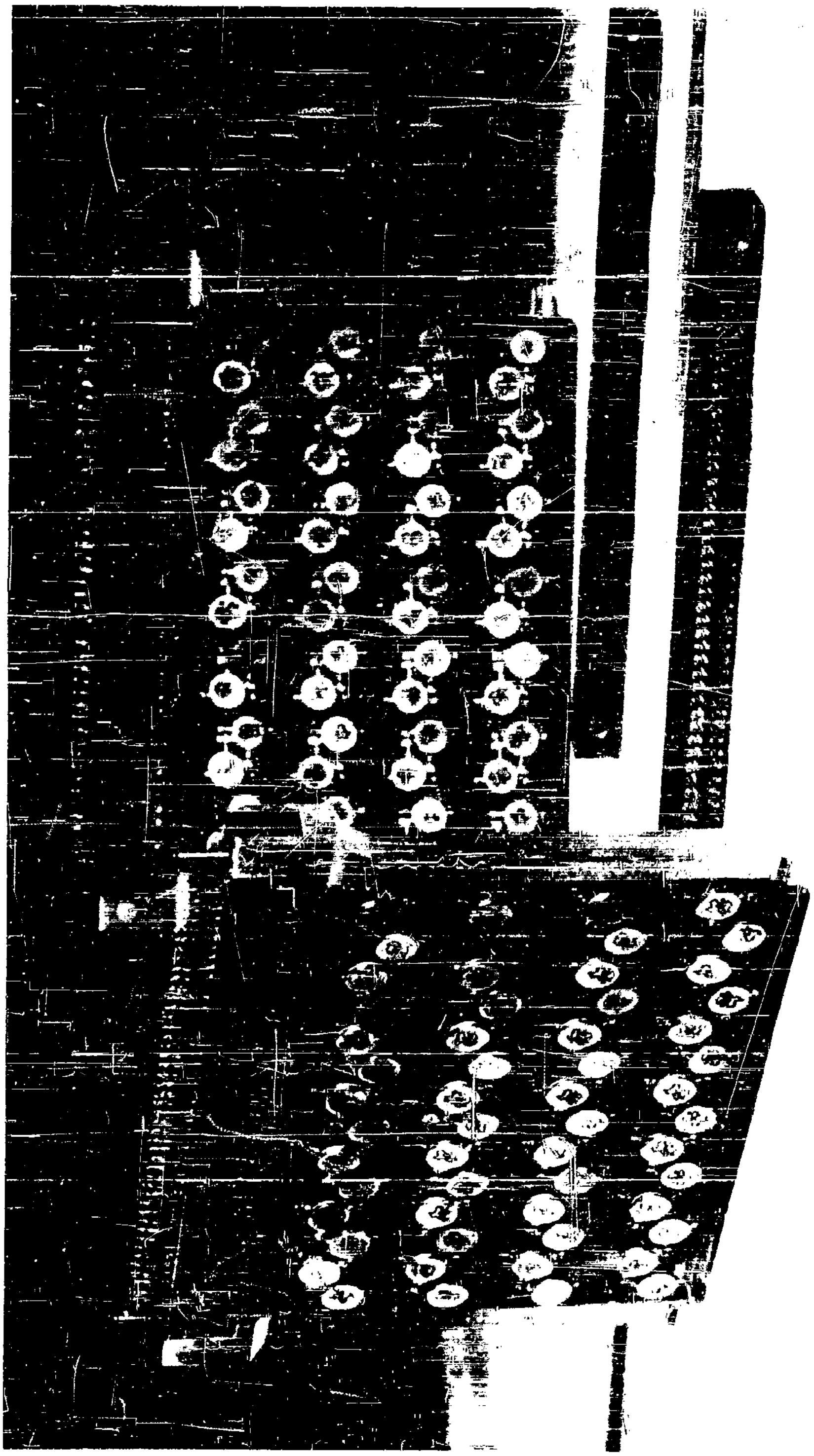


Figure 7. 56-Circuit Integrated Film Panel Pluggable Assembly

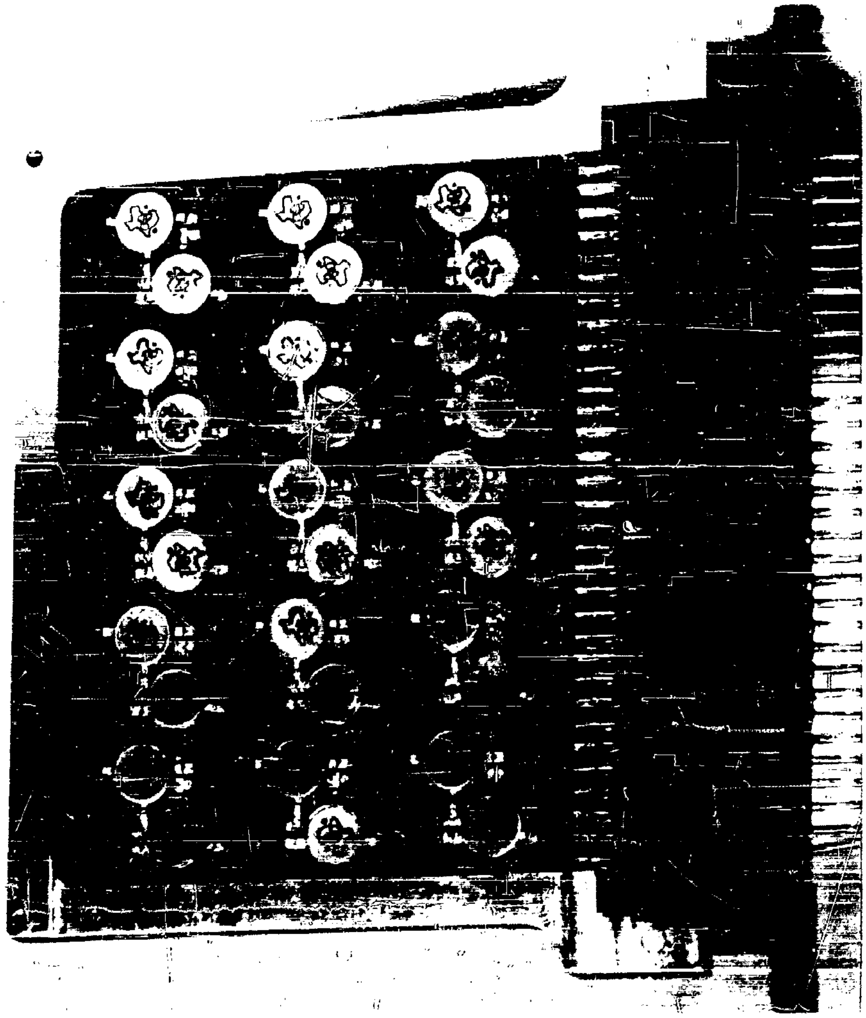


Figure 8. 32-Circuit Integrated Film Panel Pluggable Assembly

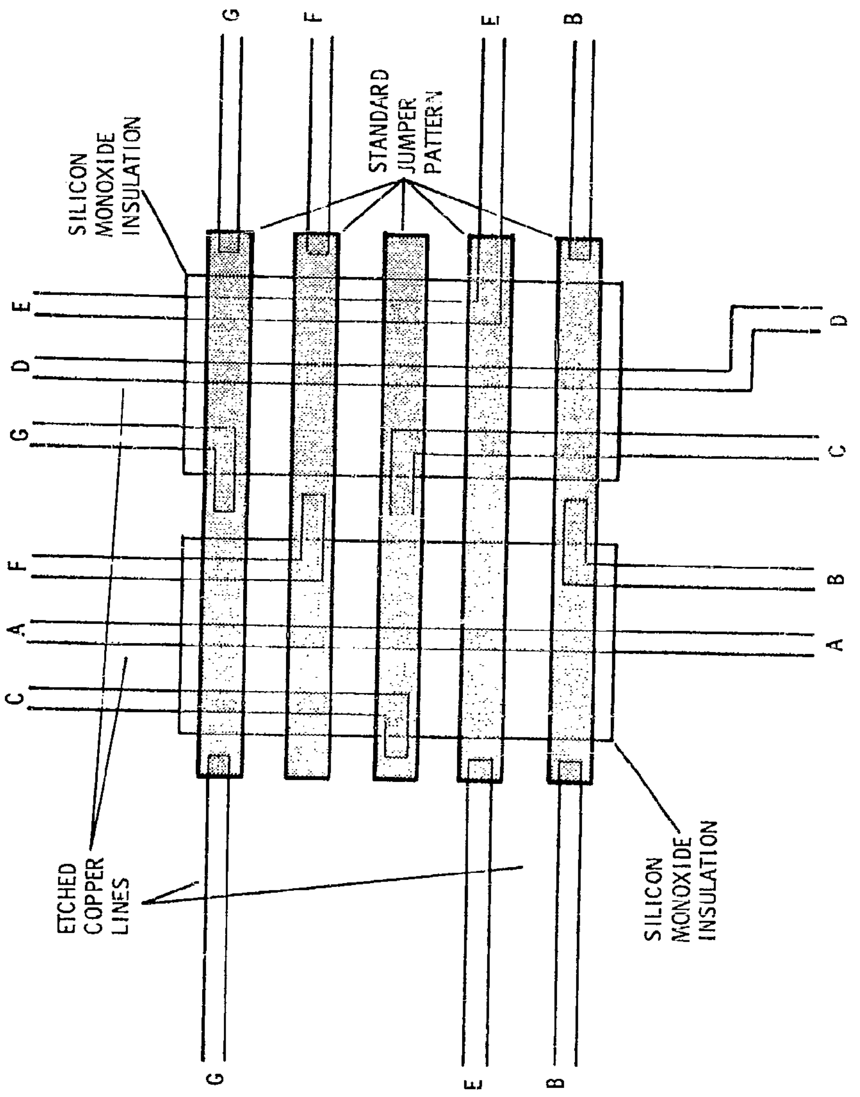

SILICON MONOXIDE INSULATION
STANDARD JUMPER PATTERN
ETCHED COPPER LINES
SILICON MONOXIDE INSULATION
G
F
E
B
E
D
G
F
A
C
D
C
B
A
G
E
B

Figure 9. Standard Film Interconnection Pattern

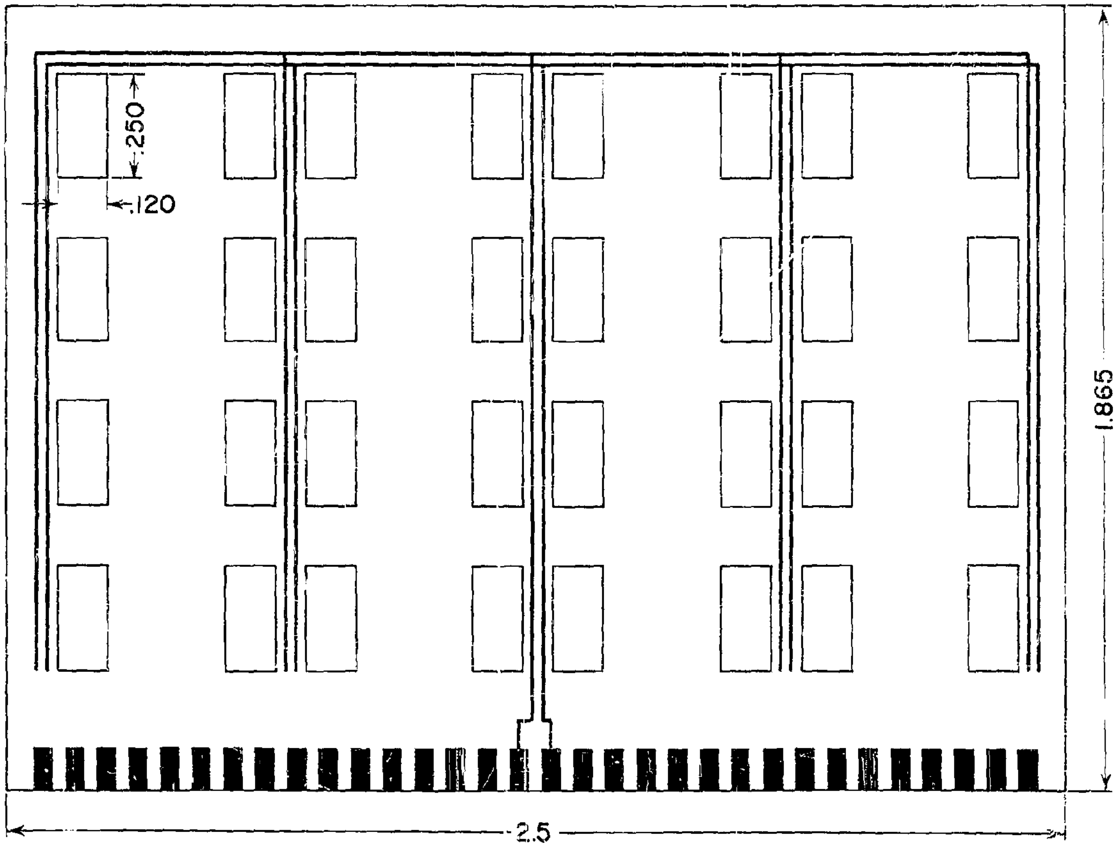

.250
.120
1.865
2.5

Figure 10. Improved Integrated Thin-Film Panel Layout

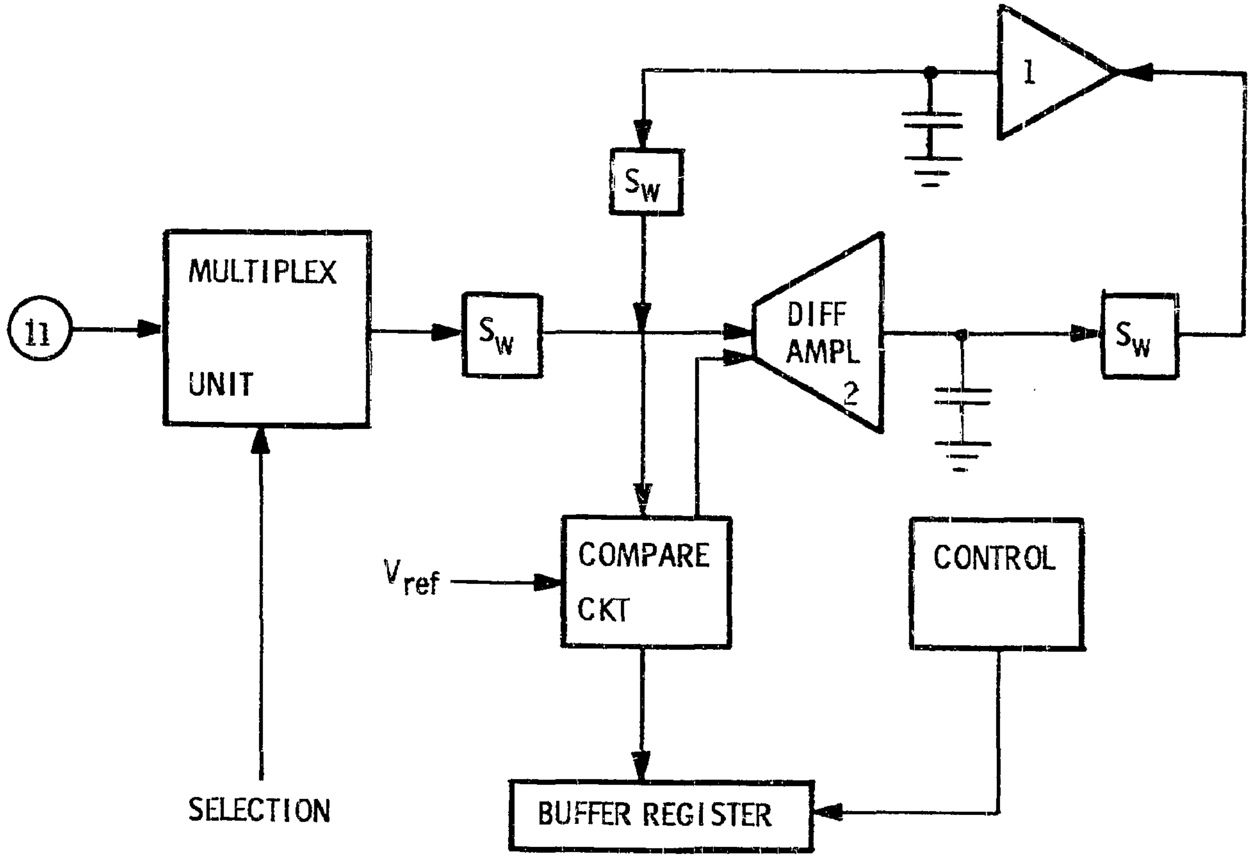

11
MULTIPLEX
UNIT
SELECTION
S_W
S_W
S_W
1
DIFF
AMPL
2
V_{ref}
COMPARE
CKT
CONTROL
BUFFER REGISTER

Figure 11. Analog-to-Digital Converter Logic Diagram

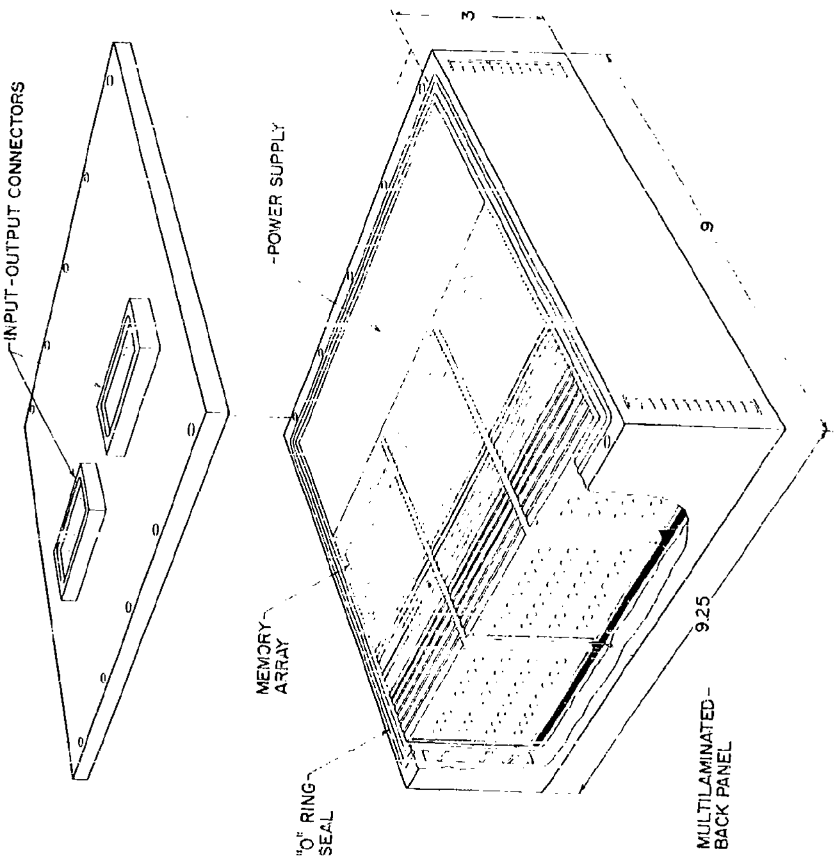

INPUT-OUTPUT CONNECTORS
POWER SUPPLY
MEMORY ARRAY
"O" RING SEAL
MULTILAMINATED BACK PANEL
3
9
9.25

Figure 12. Film Electronics Airborne Computer (Mechanical Assembly)

MATERIALS AND PROCESSES FOR THE PRODUCTION OF FILM ELECTRONIC CIRCUITRY

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Kingston, New York

ABSTRACT

This paper describes the vacuum deposition of thin film microcircuits. The fabrication of conductors, insulators and resistors will also be described as well as pilot production vacuum equipment developed for the deposition of RC-networks. The production equipment consists of four modular vacuum chambers operated as an in-line unit and equipped with mechanisms for transporting heated substrates and changing masks. The accurate registration of masks and substrates, the automatic control of evaporation sources and deposition cycles, and appropriate instrumentation promise constant output and high yield. The equipment utilizes a 3 3/4 by 5 3/16 inch substrate area. Projected yields of presently used circuitry allow for the production of approximately 7500 circuits per shift. The work has essentially been performed under contract for the Naval Avionics Facility, Indianapolis.*

******

*Part of the work reported on has been done under the following contracts:

Signal Corps Contract Number DA36-039-sc-84547
Signal Corps Contract Number DA36-039-sc-87246
U. S. Naval Contract Number N163-9142(x)

INTRODUCTION

Several new microelectronic techniques have been developed in recent years. Development programs using these techniques attempt to replace the assembly of individually produced components by the integral fabrication of complex assemblies. These integrated assemblies are expected to minimize labor cost and human error, and to increase reliability and effective component density.

Rapid developments in the field of vacuum technology indicate the feasibility of utilizing multi-layered, multi-material depositions to fabricate R-C networks and interconnect complex arrays of active elements. These thin-film techniques are applicable to the integration of bulk components with film components, as well as to the ultimate fabrication of functional all-film assemblies. Intermediate advances in microelectronics, therefore, can be combined with advances in thin-film active element development to allow an evolutionary approach to microminiaturization.

In electronic film networks, evaporated films must fulfill many new and exacting requirements. Properties which are highly structure-dependent must be utilized within close tolerances, demanding the accurate control of the deposition parameters by partially or completely automated instrumentation.

This paper describes the materials and processes used for the fabrication of integrally-deposited resistors, capacitors and interconnections with insulated crossovers, as well as the pilot production equipment developed for the U. S. Naval Avionics Facility at Indianapolis, Indiana. This effort was essentially sponsored by the BuWeps as an industrial preparedness measure. The work was performed at the IBM Laboratory at Kingston, New York.

Figure 1 shows a typical multi-circuit film panel, prior to the attachment of transistors, as produced with this equipment. The panel measures 3 3/4 by 5 3/16 inches and contains 104 transistor-resistor NOR (TRL NOR) and emitter follower circuits. The circuits are arranged in groups, permitting the large substrates to be cut into smaller panels of either 6 and 7 or 13 circuits, depending on the second level packaging approach selected. It is worth noting that 368 resistors have been simultaneously deposited within reasonable tolerances, without requiring any trimming.

MATERIALS AND PROCESSES

Resistive Films

The film resistor materials commonly used are nickel-chromium and gold palladium(1, 2, 3). Nickel-chromium has been investigated extensively and its deposition technique is well understood for sheet resistances up to 500 ohms per square. However, metal alloy resistors have two disadvantages. They cannot be obtained as stable films with high ohms-per-square values, and they tend to deposit inhomogeneously because of the different vapor pressure of the constituents.

In the past few years cermet resistor films have shown great promise both in stability and ease of fabrication. In 1959, Layer(4) reported on nitride, silicide and oxide films produced by evaporation. The chromium silicon monoxide system and a number of gold cermet systems have been explored by Beckerman and Thun(5). More recently, a process for the production of chromium-silicon monoxide resistors for integrated circuit panels has been developed(6).

In the earlier development work, chromium-silicon monoxide evaporants were deposited from two separately controlled sources. Although satisfactory process control was achieved, the method was not readily adaptable to production techniques. Furthermore, greater uniformity can be obtained from a single source of premixed cermet evaporant. Because of the large difference in the vapor pressures of chromium and silicon monoxide, precise control cannot be exercised over the composition of the deposits when both materials are vaporized from a single source containing a complete charge. This problem was solved by using the method of flash evaporation, in which a metered amount of premixed powder is delivered to a source hot enough to instantaneously vaporize both constituents. Since the densities of chromium and silicon monoxide are quite different, it has been found advisable to avoid vibrator types of powder feeds. Reliable results have been obtained using a worm-drive, powder-feed mechanism as shown in Figure 2. The premixed powder is placed in a hopper from which it is delivered by a worm gear to a free-flow orifice. The dropping powder is guided to a hot filament by a tantalum chute (Figure 3). The most suitable particle size of chromium and silicon monoxide was found to range from 325 to 400 mesh. Colloidal silicon dioxide (0.5 percent by weight) is added to reduce the agglomeration of the powder, and to improve the flow. The hot filament source consists of a 5-mil tantalum strap 1 by 1.5 inches in area which is resistance-heated to a temperature of 1800°C.

The sheet resistance of the resistors can be varied by adjusting the composition of the chromium-silicon-monoxide mixture and/or the thickness of the deposit. Figure 4 shows the practical range of resistivities as a function of composition. For the fabrication of 600 ohms per square resistors, a mixture containing 65 atomic percent chromium and 35 percent silicon monoxide is used. The resistor material is deposited through suitable mask openings at a pressure of 3-8 x 10^{-5} torr and a substrate temperature of 160°C. Conventional resistance monitoring is employed during the process. The stop value ranges from 1.2 to 1.5 times the desired final resistance value. The resistors are subsequently annealed to the desired value at 450°C in a reducing atmosphere, usually for two to five hours, depending on the initial unannealed resistance.

Dielectric Films

Dielectric materials fulfill several functions when used in film circuits. The most important of these is as insulating layers between crossings or superimposed conductor patterns, and as capacitor dielectrics. In all cases, uniformity, good adhesion to substrates and other film materials, high breakdown strength, and low dielectric losses are required. Insulator films should have low dielectric constants, whereas high constants are preferred for condensor dielectrics(7). Because of the small film thickness used, however, the latter requirement is not paramount. In TRL circuitry, the annealing temperature of 450°C, used with present resistor materials, restricts the choice of dielectric materials to inorganic compounds.

In spite of its not very well defined stoichiometry, silicon monoxide offers advantages over other film dielectrics studied(8). It condenses in an amorphous form indicating a very low surface mobility even at elevated temperatures. Due to this low mobility, silicon monoxide forms an ideal undercoating for the circuit network by effectively smoothing out minor surface irregularities. The underlayer also acts as a barrier against ion migration from the substrate.

Silicon monoxide has similar or superior properties as a protective coat when compared with such materials as magnesium fluoride or rare earth fluorides and oxides. It is employed to advantage particularly in those cases where silicon monoxide is already used as a dielectric and insulating material, since this minimizes the required number of coating materials.

The dielectric constant and breakdown strength of silicon monoxide are dependent on deposition parameters. The accepted value of the dielectric constant is 6.0. Film thicknesses ranging from 5000 to 30,000 Å allow capacitance values from 7 x 10^{-2} to 1.5 x 10^{-2} µf per cm^2 of area. Dielectric constants from 4 to 10 are obtainable by varying the deposition rate and oxygen content of the films. However, increasing oxygen content tends to make the films hygroscopic and thus electrically unstable. The breakdown strength of silicon monoxide falls into the range of 2 x 10^6 volts per centimeter, resulting in adequate insulation for most circuit applications.

Silicon monoxide is best evaporated from a hollow crucible source at a pressure of 5 x 10^{-6} torr or lower. Because of the porous nature of the raw material, care must be taken to outgas the charge prior to evaporation, and to evaporate at a rate which is slow enough to prevent the ejection of particles from the source onto the substrate. Figure 5 shows the hollow crucible source design, such as described by "Drumheller" (9). The hollow perferated cylindrical filament is surrounded by the evaporant material, which is vaporized, the vapor stream passing through the perforations and up the chimney to the substrate. Particle ejection is further minimized by charging the crucible only with particles larger than 20 mesh.

Silicon monoxide films show minimum mechanical stress (10) when deposited at source temperatures between 1300 and 1400°C and substrate temperatures above 300°C. These temperatures produce a well adherent and durable film. Especially developed instrumentation controls the deposition rate within 5 percent.

Useful film thicknesses range from 5,000 to 25,000 Å. Because of the low surface mobility of silicon monoxide, the edge contour of deposited SiO areas is relatively abrupt. In order to soften this contour, a controlled mask-to-substrate distance of two to five mils is used, resulting in a more gradual slope and an increased yield of conductor cross-overs.

Conductive Films

Terminal lands and electrical interconnections are made with copper. Copper not only provides good electrical properties and acceptable film-to-film joints, but also lends itself well to conventional etching techniques which might be employed, in addition to masking, as part of the pattern-forming process.

Intermittent wire-feed sources have proven to be unacceptable because of continuous outgassing, spitting, and particle ejection from the source material. Therefore, a radiantly-heated crucible source, which can be thoroughly outgassed prior to film deposition, has been developed. This crucible, shown in Figure 6, not only gives smoother films but also allows the use of the ionization gauge rate monitor(12, 13) for evaporation control.

Due to the higher mobility of copper at elevated temperatures, films deposited at substrate temperatures higher than 170°C tend to crystallize in a randomly-oriented fashion, and have rough surfaces which are difficult to insulate. Copper films deposited below 170°C are quite highly oriented with the [111] crystallographic direction perpendicular to the substrate. Since growth is a function of crystallographic direction, an even growth perpendicular to the substrate occurs in this case and a smooth, readily insulated film results. Figure 7 shows the results of laboratory experiments relating the substrate temperature to the crystal structure of the film. It is apparent that the critical temperature needs to be maintained only during the nucleation of the film, and that subsequent temperature rises due to radiant heating by the source have no adverse effect on the quality of the films.

Good adhesion of copper films is achieved by depositing an underlayer of chromium a few hundred angstroms thick. This technique, coupled with the stress relief which occurs during subsequent insulator depositions at 300°C(11), assures a high quality, adherent, conductive film.

PRODUCTION FACILITY

In the vacuum deposition of film networks, two basic approaches are used. One is a "closed cycle process" utilizing a mask-source or mask-substrate changing mechanism. This approach facilitates the evaporation of different materials, and the changing and accurate registration of a series of masks and substrates, all in one pump-down cycle. The desired substrate temperatures, deposition rates and, in certain cases, film thicknesses are selected manually, but controlled automatically during the process.

The second approach consists of a "batch coating" process where each material is deposited in a separate system during one pump-down cycle. Although masks and substrates are changed manually, this process does permit simultaneous deposition on a large number of circuits and avoids the cross contamination of evaporant materials.

The production facility designed and built at Kingston combined the cleanliness of the batch-coating process with the reduced pumping time of the semi-automated closed-cycle process. Maximum system flexibility is accomplished by a modular design which allows the interchange of source chambers and control panels with a minimum of rearrangement.

Figure 8 shows a photograph of the complete modular in-line system. Its general features are given in Table I.

TABLE I - System Characteristics

System Design

- Modular construction
- Four deposition chambers, source chambers and pumping systems
- Vacuum locks at entrance and exit magazines
- Controls in one panel assembly
- Expansion capability
- Conversion to batch operation

Table I - continued.....

Process Capacity

24, 3.75 x 5.18 in^2 substrates
6 masks per chamber

Estimated Output - 1963

900 square inches per 8 hour shift

Vacuum System

The majority of depositions should be done at vacuum pressures in the lower 10^{-6} torr range. The pumping system must be capable of high pumping speeds in this range, and an ultimate pressure in the 10^{-7} torr range since substrate heaters, large-area, hot-crucible sources, gassy-powder evaporants, and internal chamber mechanisms all contribute to the gas load. To reduce the load on the pumping system, the volume to be evacuated was held to a practical minimum by mounting the pumping components close together and keeping the chamber size of each module small. Each main chamber (Figure 9) is pumped with a 4100 liter per sec. oil diffusion pump, and backed by an 80 c.f.m. mechanical pump. High-conductance components and oversize interconnecting pipe further aid pumping. In initial tests, the unbaked system was evacuated to 5×10^{-6} torr in 12 minutes and to 4.5×10^{-7} torr in 2 hours. No valves are built into the main chambers, thus allowing chambers of a different size and shape to be used if needed to satisfy future requirements. All valves are electro-pneumatically operated by push buttons located on the control panel.

A multi-coolant baffle is placed between the diffusion pump and main valve to minimize back-streaming of the pump oil vapors. The temperature of this baffle is maintained at -80°C (-175°F) by a commercial three stage refrigeration system. Even a single-stage refrigeration unit, when used with a good trap design and the new high-speed diffusion pumps, is very effective in reducing back-streaming.

Mechanical Operation

The fabrication of multiple-layer, thin-film components requires the precise positioning of masks and substrates in relation to each other and in relation to source and monitor equipment. In addition to accurate registration, the design of a transport and mask-changer mechanism must also provide for the storage and handling of additional masks and substrates, the moving of substrates from one deposition station to the next, and an indication to the operator of the position of the mechanism. Parts must move freely without lubrication and, in most cases, at elevated temperatures. This was achieved by providing large clearances or by using stainless steel ball bearings.

Even the simplest mechanism in a vacuum chamber can be the source of a virtual leak. There are many places where gas can be trapped and pumping impeded. These obstructions to vacuum pumping are reduced by providing vents in blind holes, hollow or slotted dowel pins, and slotted screw threads. Large flat mating surfaces are designed with grooves or relief cuts.

A schematic of a 4-station, in-line, modular system is shown in Figure 10. The operating mechanism can be divided into three major areas: substrate magazines, substrate transport, and mask changer.

Substrate Magazine

The substrate magazines are located at either end of the system and serve as load and unload stations. A high vacuum valve between a magazine and its adjacent chamber allows for loading and unloading without breaking the vacuum in the main chambers. The magazines have a 24 substrate capacity, stacked vertically as shown in Figure 11. The magazine mechanism is actuated by the substrate transport mechanism in the adjacent chamber. Each time a substrate is moved into the first chamber, a new substrate is lowered into location and preheated. The exit magazine is of similar design and also serves as a cooling station.

Substrate Transport

The substrate transport mechanism consists of four modular assemblies, one for each chamber (Figure 12). The in-line arrangement of the chambers results in a continuous transport mechanism, which removes the substrate from the entrance magazine, transfers it through the four deposition stations, and places the finished substrate in the exit magazine.

The substrate transport mechanism consists of a motor-driven ball screw with attached carriage and pick-up bars. The motor drives the carriage in a forward-return motion. As the carriage moves back, the pick-up bars slip past the substrate holder. Engagement with the substrate holder takes place on the return motion moving the substrate 7 1/2 inches to the next position. Since the motor is mounted inside the vacuum chamber, it was modified for vacuum service by a complete degreasing, replacing the stator coil insulation with glass lacing cloth, and cutting vents to facilitate outgassing.

Each chamber has its own radiant heater assembly and control. The upper heater sections run the full length of the four chambers. The lower sections have openings at each evaporation station.

Mask Changer

The chambers are equipped with identical mask changers. The motor driven mask changer (Figure 13) removes a clean pre-heated mask from the mask cartridge and engages the mask with the substrate within an accuracy of 2 mils.

At the termination of a deposition, the mask is disengaged but not returned to the cartridge. After a pre-determined number of depositions, the used mask is returned to the cartridge and a new mask removed. Indicating lights show the mask position and the number of depositions made through the mask presently in use. The mask cartridge, containing six masks, is removable and serves as a container for transporting masks away from the system.

Each chamber has its own modular control panel which includes the vacuum instrumentation. Ionization and thermocouple gauges monitor the vacuum conditions at several stations in the chamber and pumping system. Protective circuitry automatically closes the necessary valves and turns off the diffusion pumps in case of electrical or water-pressure failures.

All movement of the substrates and masks within the chambers is controlled by the operator from the control panels. Electro-mechanical interlocks are provided to prevent damage to the system due to faulty operation. Substrate temperatures are monitored and controlled by thermocouples located in the heater housing.

The evaporation rate of the silicon monoxide is controlled by an ion-gauge rate monitor(12-13). The sensing element (Figure 14) consists of a filament, anode and collector. The vapor stream is ionized and discharged at the collector. The collector current is nearly proportional to the density of the stream. The pressure-compensated, sensing-element output is fed to a control unit which, by adjusting the source power, maintains the desired evaporation rate. The desired film thickness is obtained by closing a timed shutter. The use of a heated collector to constantly re-evaporate the deposited material assures a constant sensitivity during its operation.

The resistance of the cermet resistors is monitored directly on separate monitoring substrates. As the mask and substrate holders are engaged, spring-loaded contacts connect the resistor monitor terminal lands to an external circuit, which closes the shutter when the desired resistor value is reached.

OPERATIONAL EXPERIENCE

The production equipment has been operationally tested for a number of weeks, using the materials and processes described previously. The operation of the vacuum system, transport mechanism, mask changers, control circuitry and sources has been evaluated in detail.

The pumping equipment and vacuum instrumentation has been found to operate in a satisfactory manner. Pumping time from atmospheric pressure to 5×10^{-6} torr in 12 minutes. Pressures of 5×10^{-6} torr have been maintained with all heaters and sources operating simultaneously. When it is necessary to bring a magazine or source chamber to atmospheric pressure for servicing, the system can be pumped down again to 5×10^{-6} torr in 2 minutes.

After initial mechanical adjustments the entrance and exit magazines, transport mechanisms and mask changing mechanisms have operated without fault during test runs simulating an output of 48 consecutive substrates.

Because of the limited operational experience, firm yield figures are not available at this time. However, a preliminary evaluation of about forty panels, containing the circuit shown in Figure 1, has demonstrated that the circuit design requirements relative to film quality, thickness and uniformity have been met. The deposition of 600 ohm-per-square resistors was accomplished in about three minutes, with a distribution of ±10 percent over the substrate area which contained 368 resistors. The resistors have been annealed without difficulty after the removal of the fully-coated substrates from the exit magazine.

Copper has been deposited at a rate of 30 Å per sec. with a distribution of ±4 percent over the 3.75 by 5.18 inch substrate area. The reproducibility of the target thickness of 10,000 Å is +20 percent -0 percent. The incorporation of an improved source design into the system should ultimately result in deposition rates approaching 100 Å per second at the 26-inch source-to-substrate distance. Silicon monoxide has been deposited at rates up to 35 Å per second with a distribution of ±6 percent over the substrate area. The reproducibility of the target thickness of 20,000 Å is ±5 percent. Laboratory experiments with specially prepared ultra-pure, silicon monoxide have shown that rates approaching 120 Å per second are possible.

The cycle time achieved during these first runs is about six hours for the completion of 24 substrates. This cycle time can be nearly halved by incorporating known source designs and available materials of higher quality. It is expected that an ultimate cycle time of two hours will be obtained.

Experience in vacuum tube and semiconductor manufacture has shown that when production quantities of components are fabricated under the discipline of quality control procedures, using specially designed process control instrumentation, increased yields and lower costs are obtained. The transition of vacuum-deposited thin-film technology from laboratory to production will mark another major step in microelectronics and the everexpanding role of computer applications in the Space Age.

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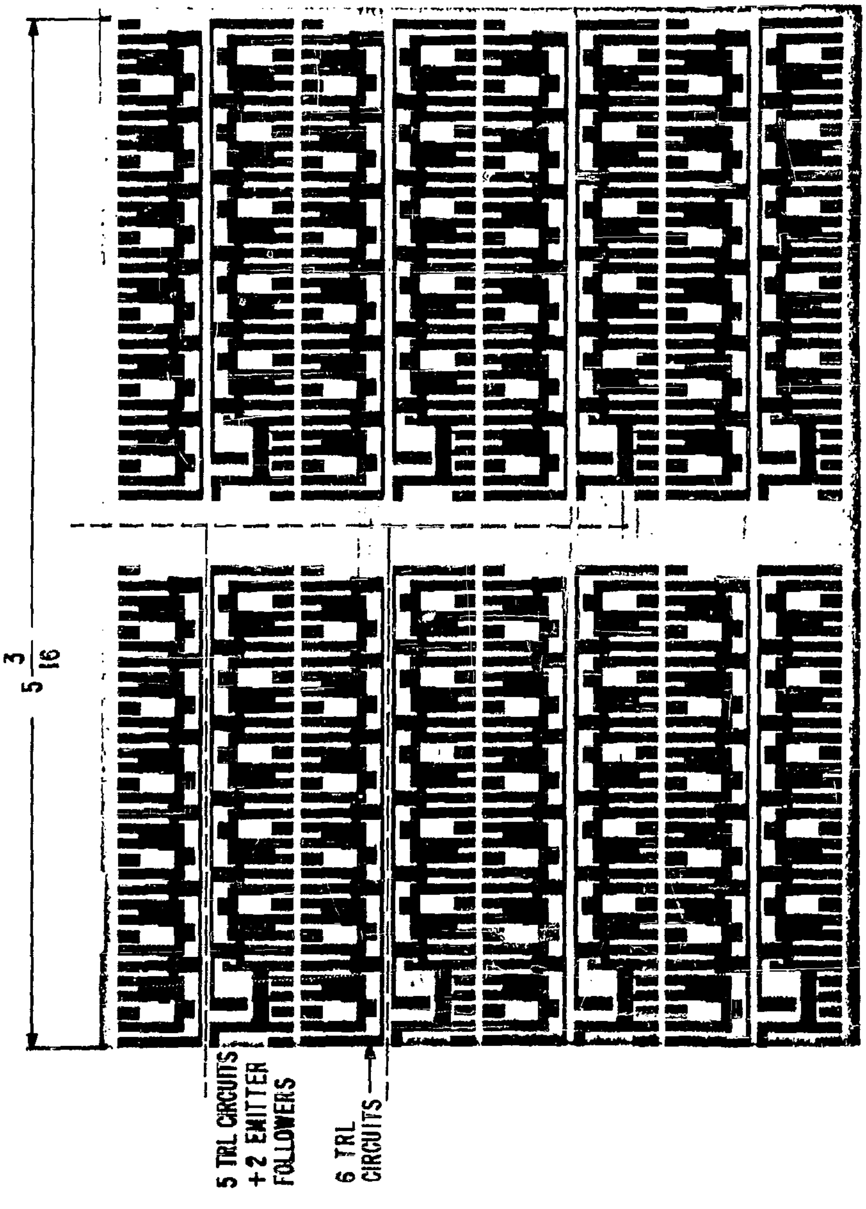

$5\frac{3}{16}$
5 TRL CIRCUITS +2 EMITTER FOLLOWERS
6 TRL CIRCUITS

Figure 1. Typical Circuit Pattern

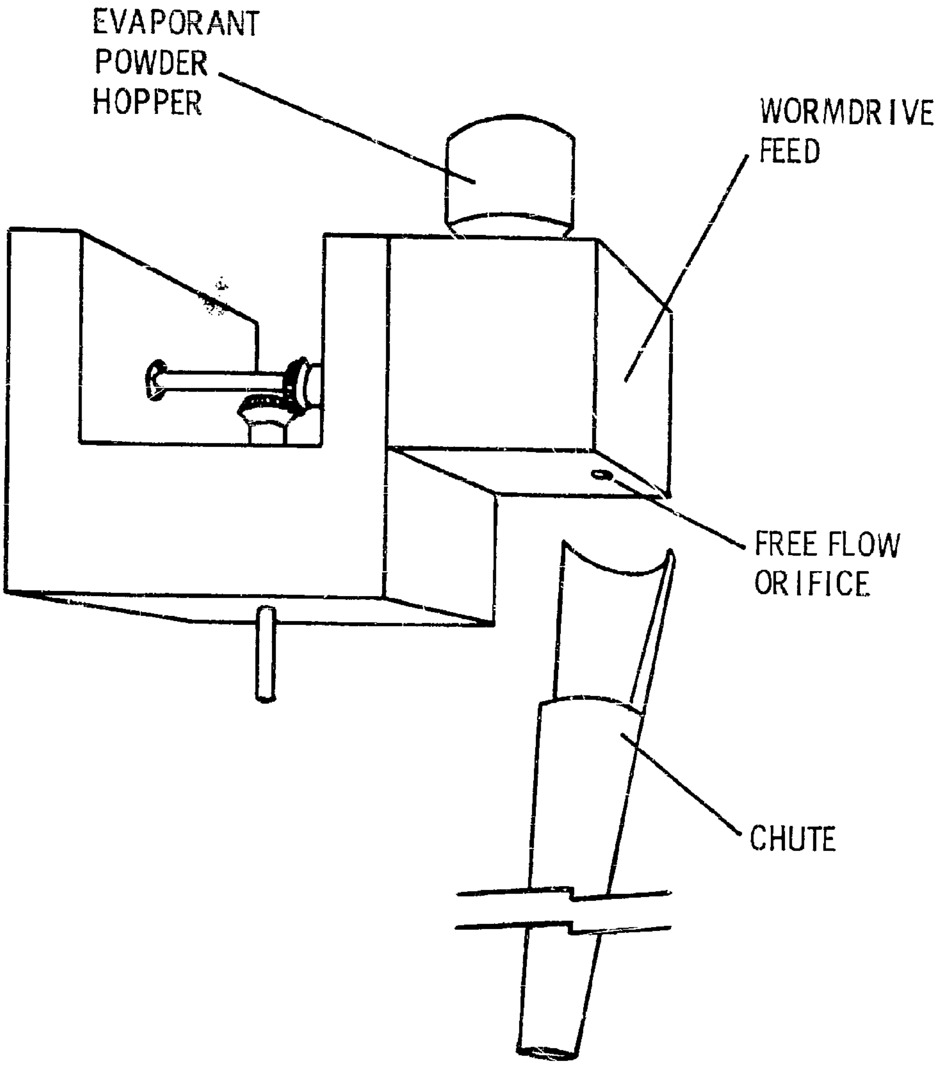

EVAPORANT POWDER HOPPER
WORMDRIVE FEED
FREE FLOW ORIFICE
CHUTE

Figure 2. Worm-drive Powder Feed

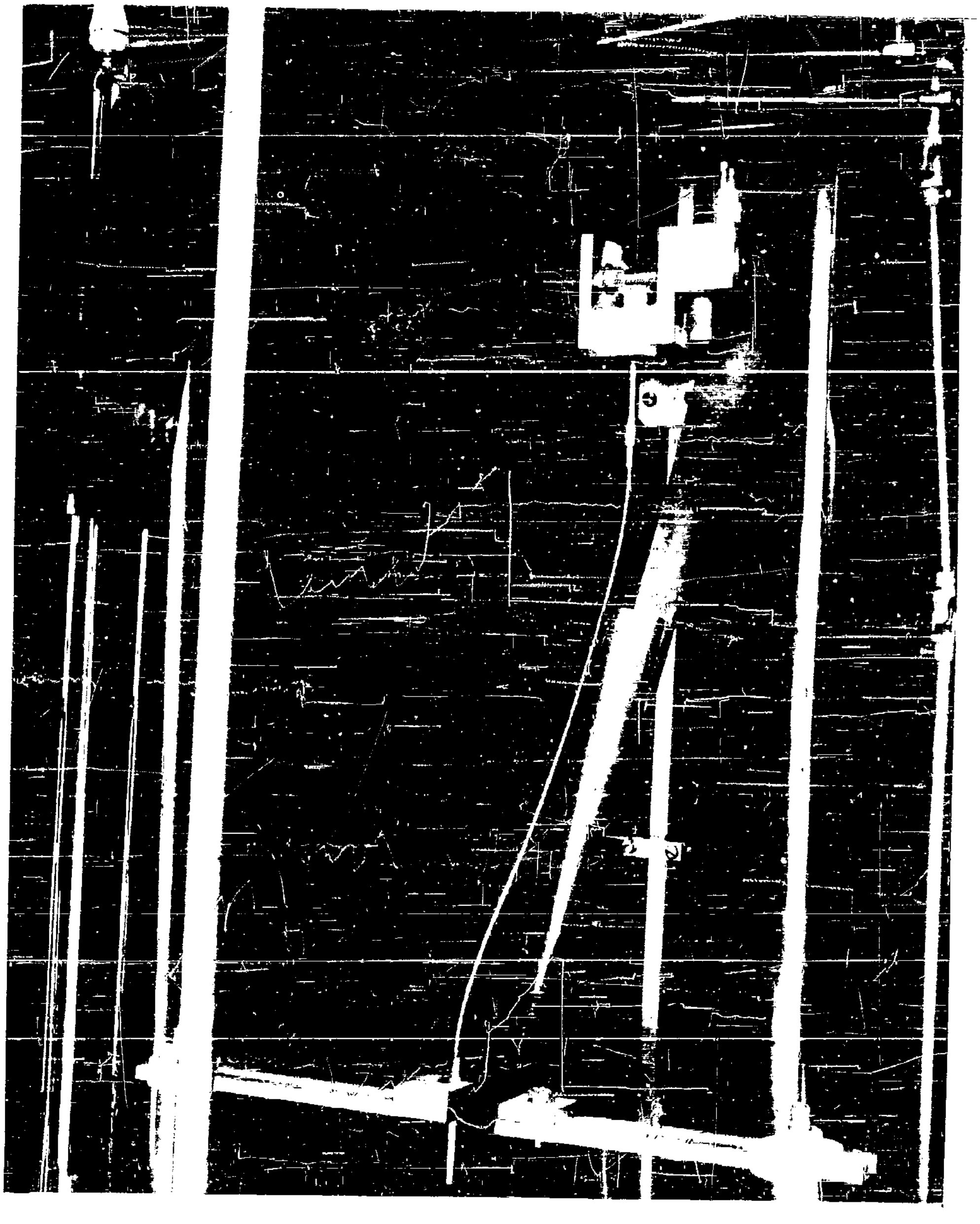


Figure 3. Powder Feed Source Arrangement

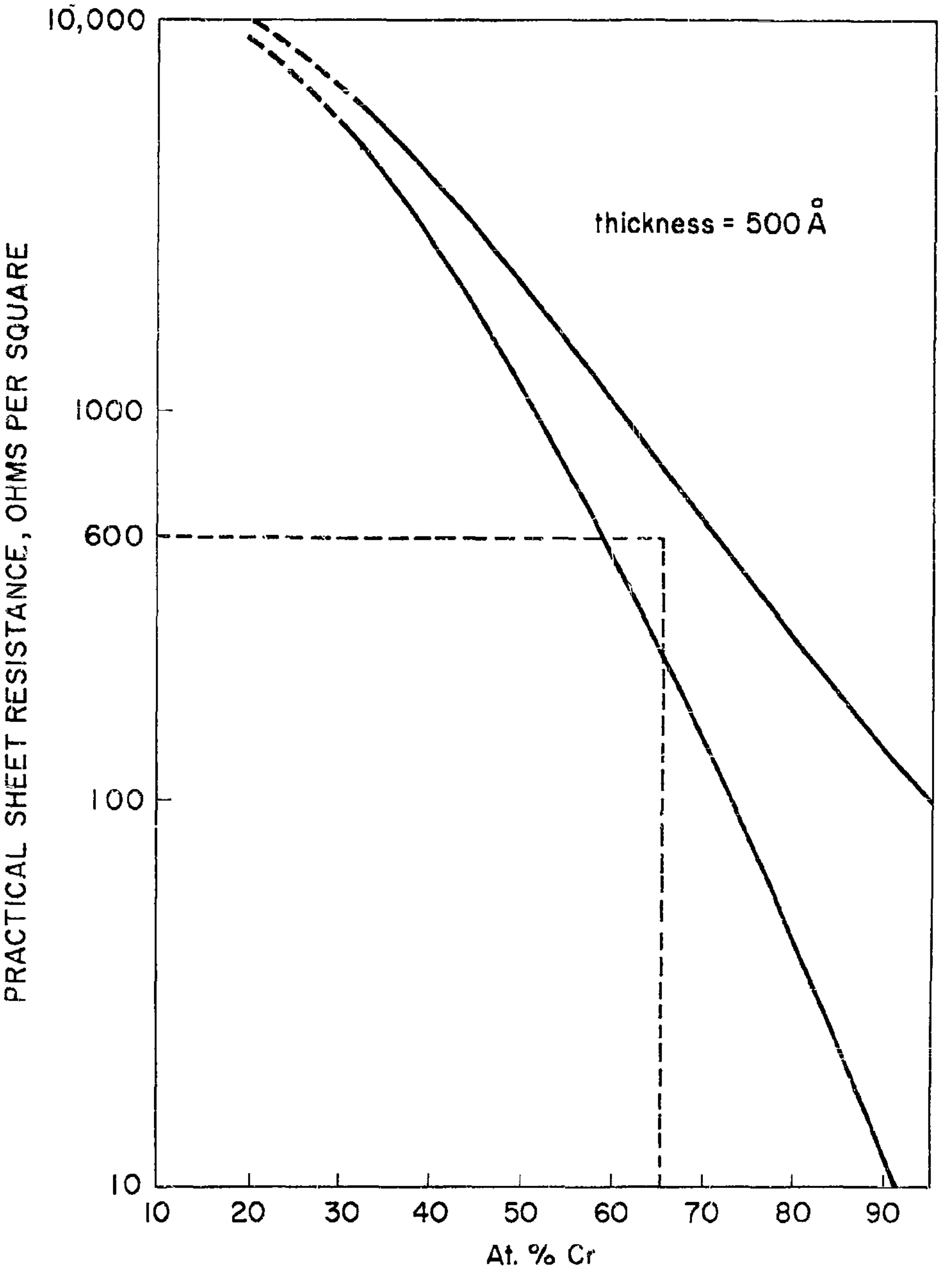


Figure 4. Resistance vs. Composition

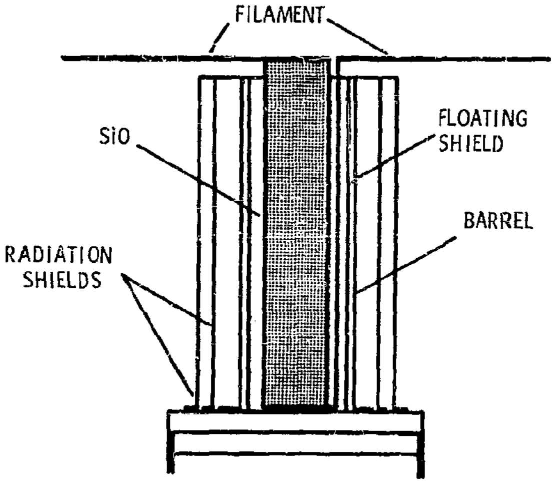

FILAMENT
SiO
FLOATING SHIELD
BARREL
RADIATION SHIELDS

Figure 5. Hollow Crucible Source

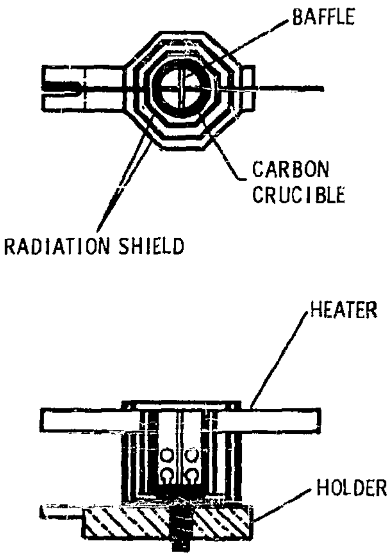

BAFFLE
CARBON CRUCIBLE
RADIATION SHIELD
HEATER
HOLDER

Figure 6. Crucible Source for Copper

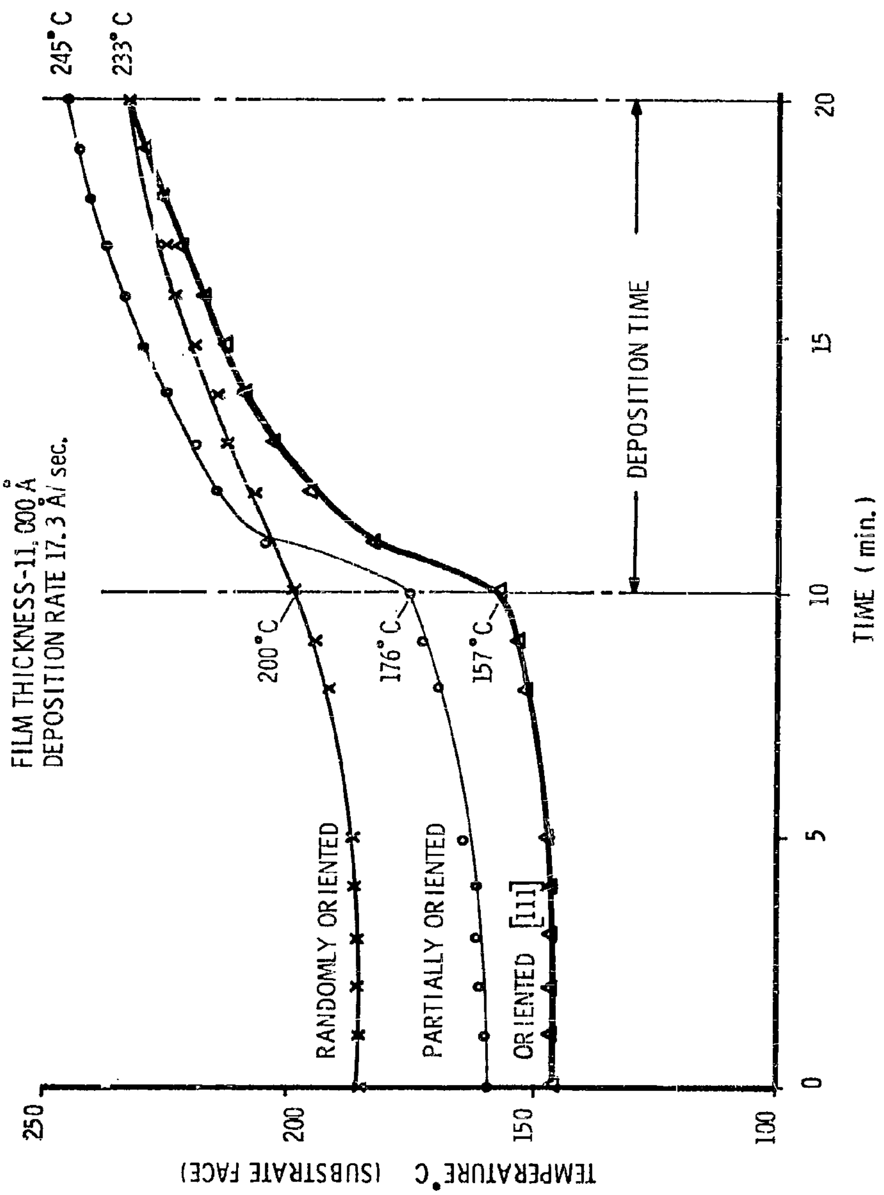


Figure 7. Substrate Temperature vs. Film Crystal Structure

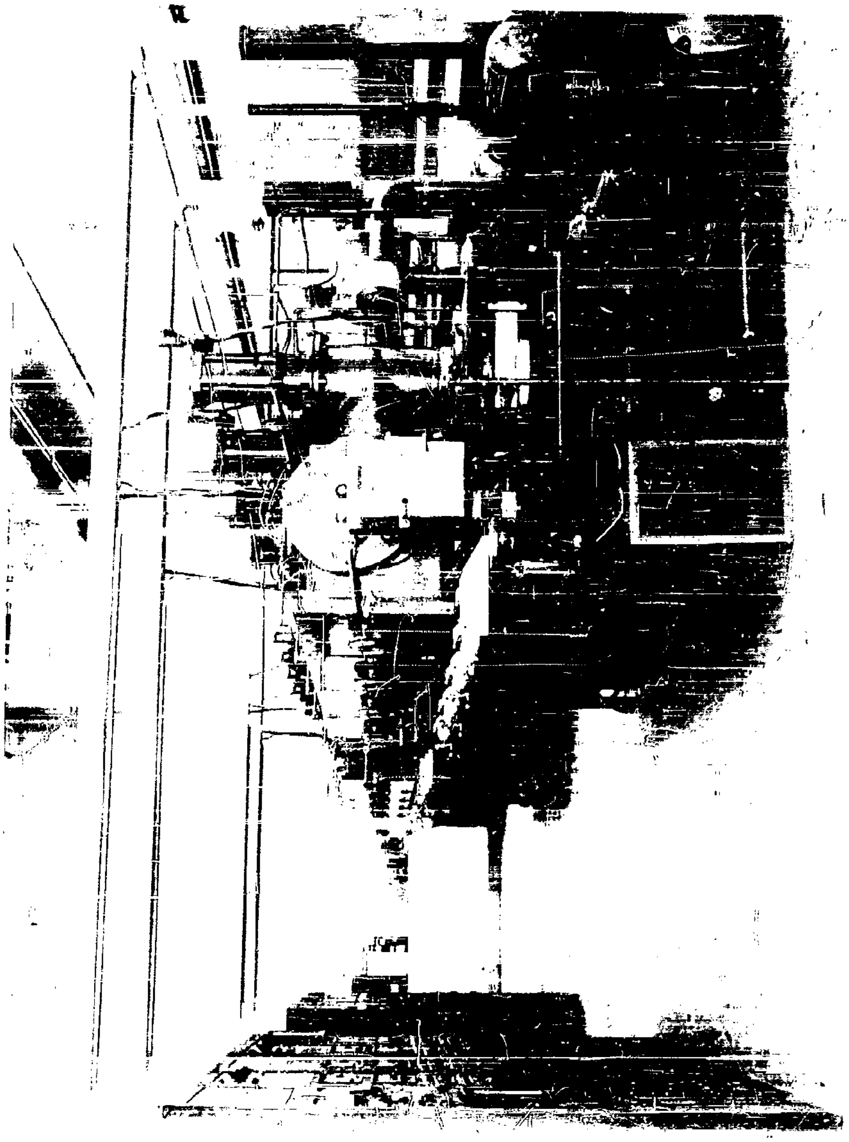


Figure 8. Modular In-line System

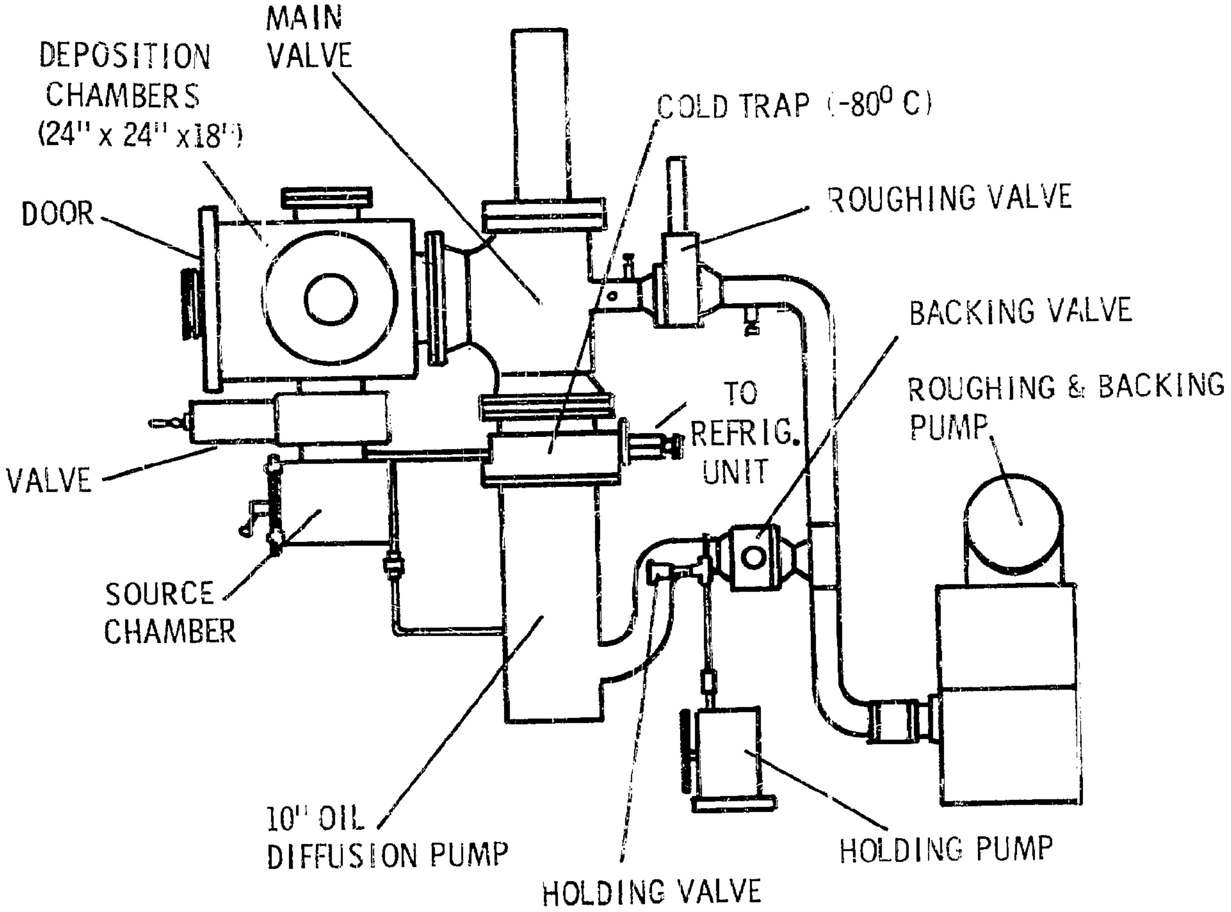

MAIN
VALVE
DEPOSITION
CHAMBERS
(24" x 24" x18")
DOOR
VALVE
SOURCE
CHAMBER
COLD TRAP (-80° C)
ROUGHING VALVE
BACKING VALVE
ROUGHING & BACKING
PUMP
TO
REFRIG.
UNIT
10" OIL
DIFFUSION PUMP
HOLDING VALVE
HOLDING PUMP

Figure 9. Schematic of a Single System

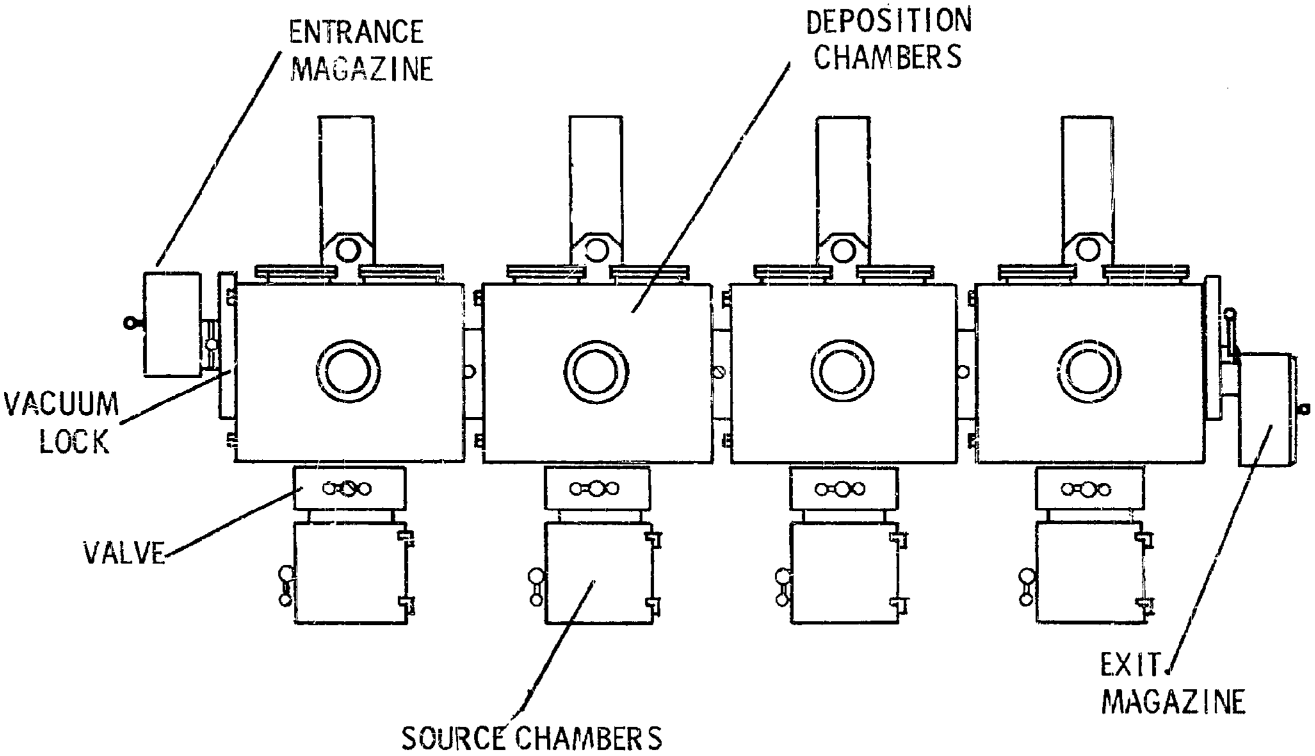

ENTRANCE MAGAZINE
DEPOSITION CHAMBERS
VACUUM LOCK
VALVE
SOURCE CHAMBERS
EXIT MAGAZINE

Figure 10. Four-station, In-line Modular System

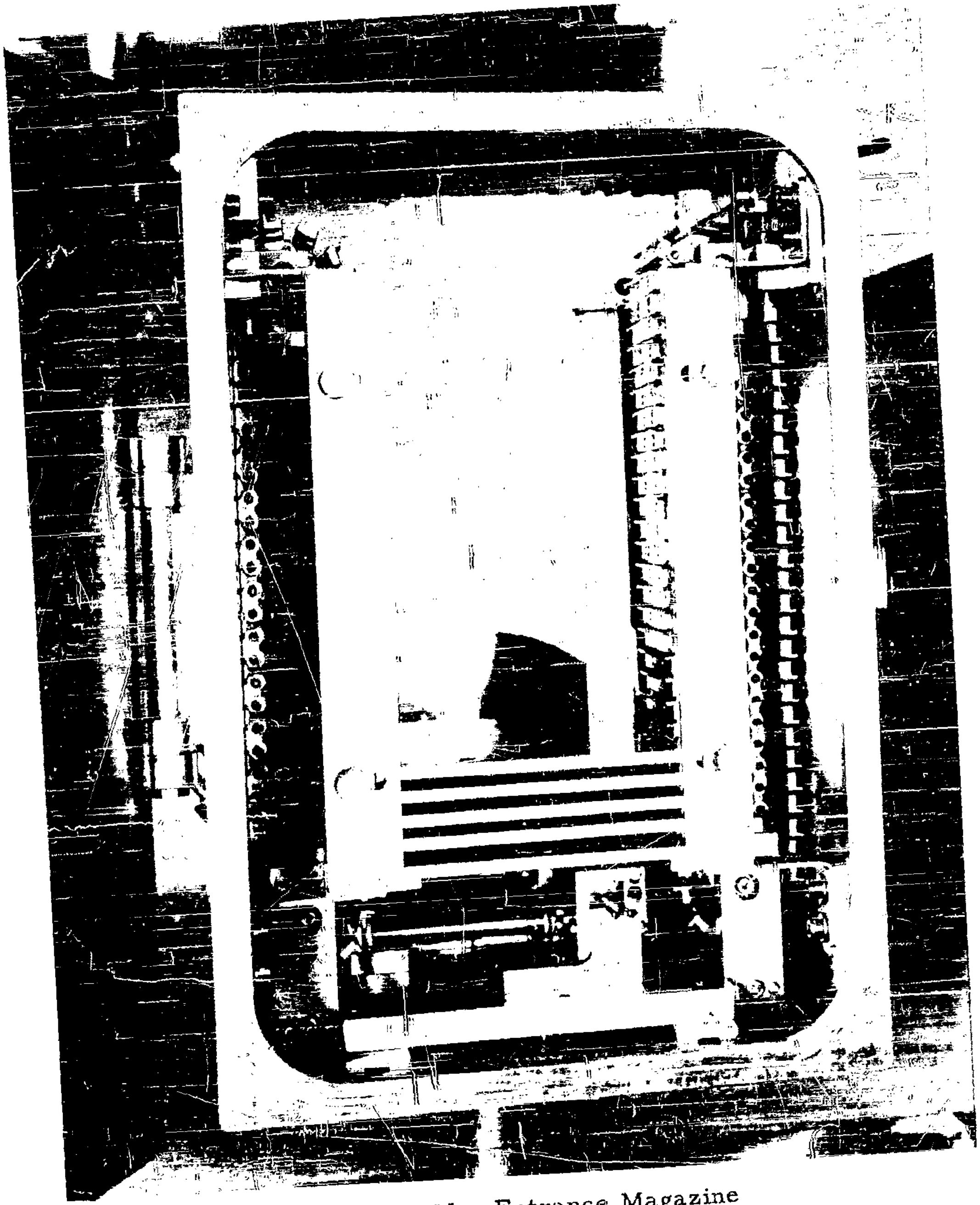


Figure 11. Entrance Magazine

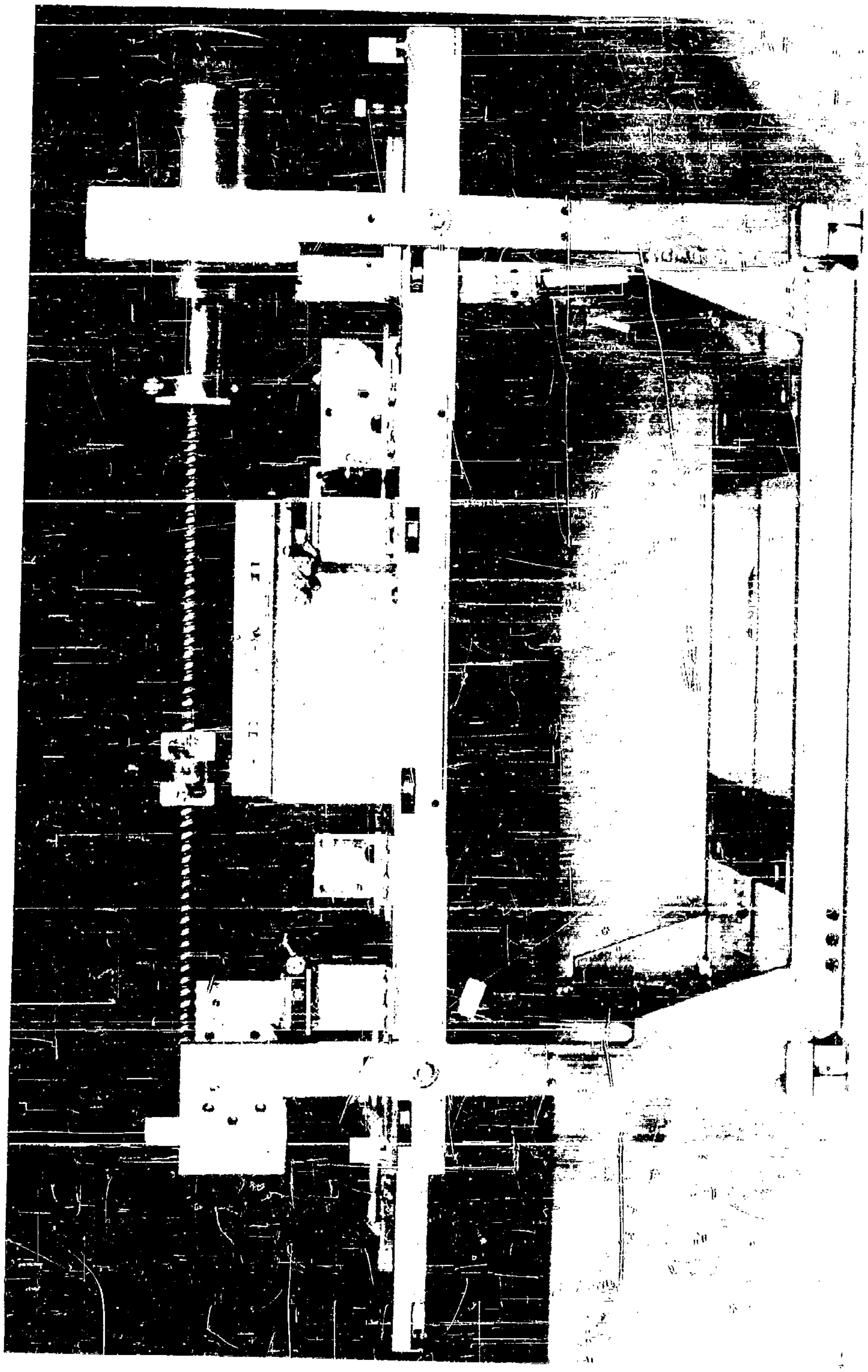


Figure 12. Substrate Conveyor Assembly

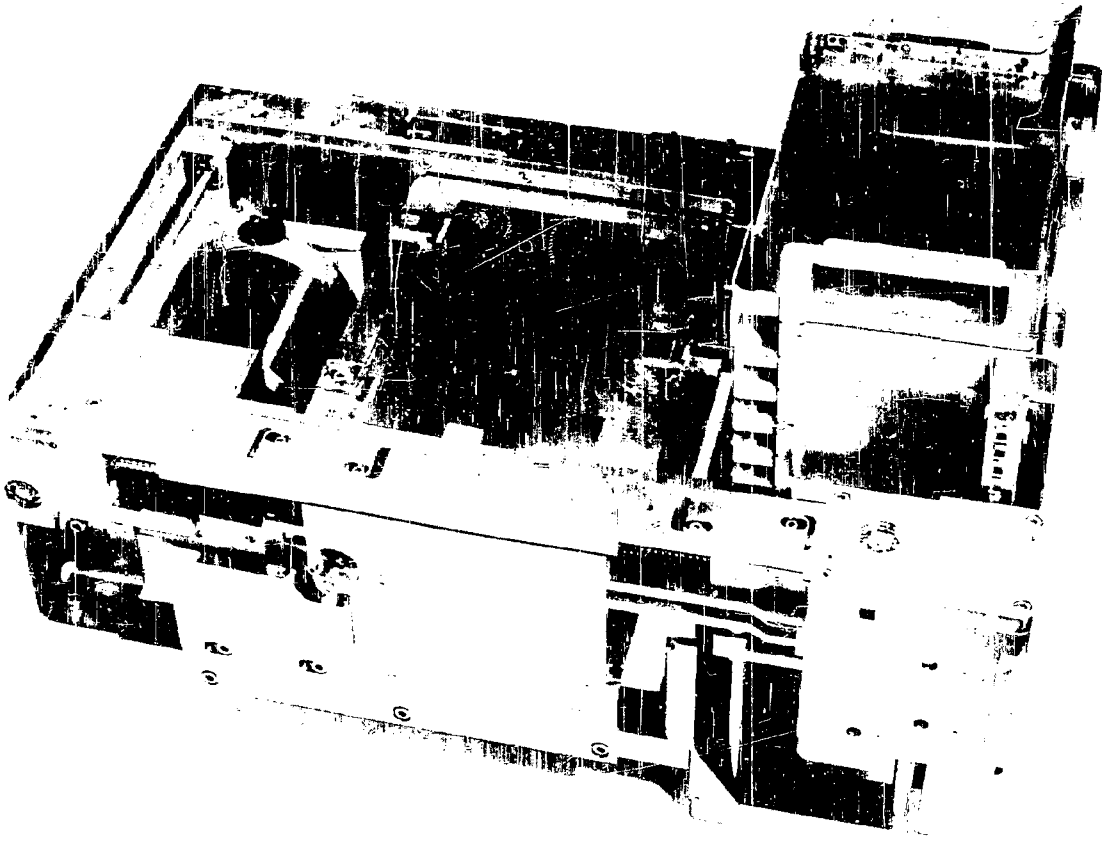


Figure 13. Mask Changer

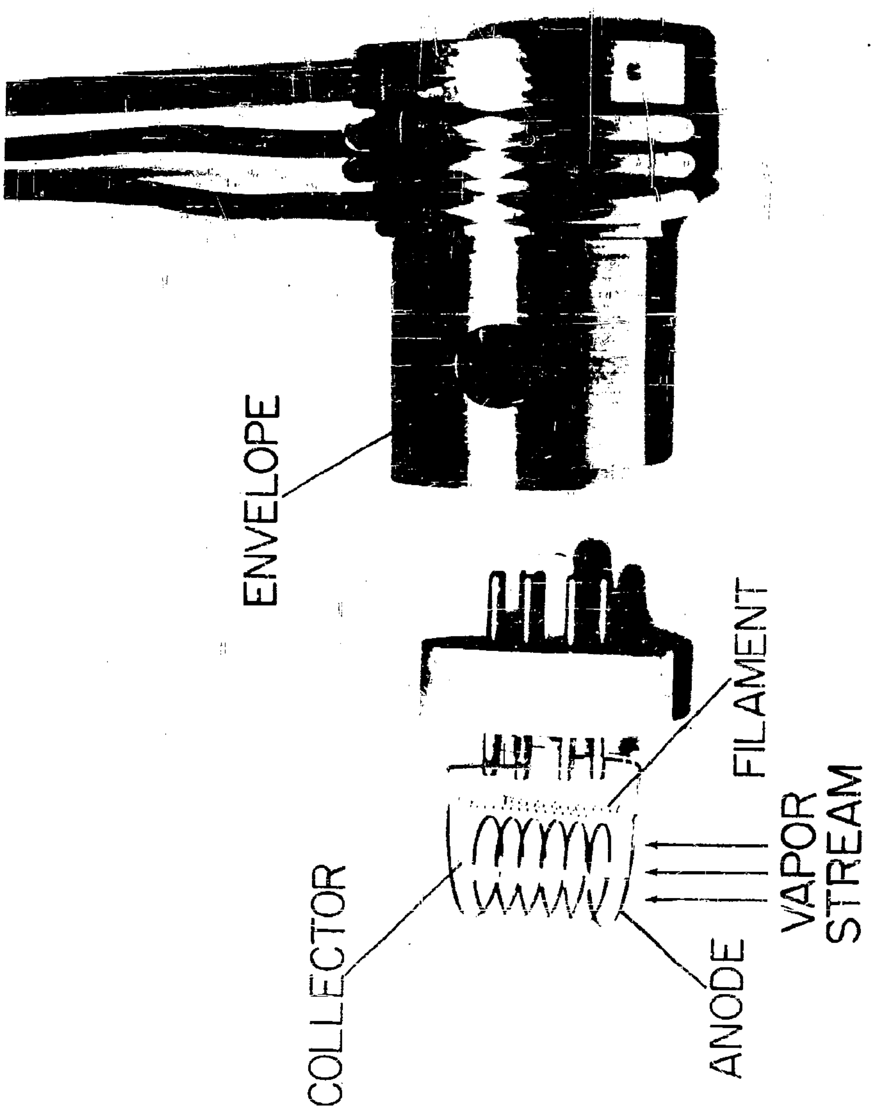

ENVELOPE
COLLECTOR
FILAMENT
ANODE
VAPOR STREAM

Figure 14. Sensing Element of Ion Rate Monitor

A FREQUENCY MODULATED PHASE-SHIFT OSCILLATOR

Charles Feldman and Harry E. Culver
Melpar, Incorporated
Falls Church Virginia

1. INTRODUCTION

The ultimate goal of Melpar's thin film program is to acquire knowledge for the fabrication of complete thin film integrated circuits capable of operating to 500° C and possessing a high degree of radiation resistance. Effort has been concentrated on the preparation and properties of materials capable of operating at high temperatures and studying the various physical phenomena and effects in these materials that may lead to circuit functions. Studies have thus been conducted on surface phenomena and anomalies found in films. The present paper is divided into two parts, the first part will give a very brief summary of the materials and effects currently being studied; and the second part, will deal with the use of these materials in an actual circuit. It must be emphasized that the chief purpose in describing the circuit is to illustrate the phenomena and materials used and in no way should be construed to indicate that the basic material studies have come to an end.

2. MATERIAL AND EFFECT STUDIES

2.1 Metal Films

Work on metal film resistors over the past year still confirms the fact that rhenium forms a very suitable film resistor which is capable of operating to 500° C.(1) Figure (1) shows a rhenium film resistor operating at 12 watts at a temperature of 850° C. Due to the difficulty of soldering to rhenium, the pad or land areas, for purposes of intermediate circuit studies, consist of deposited gold or copper layers alloyed to the rhenium film.

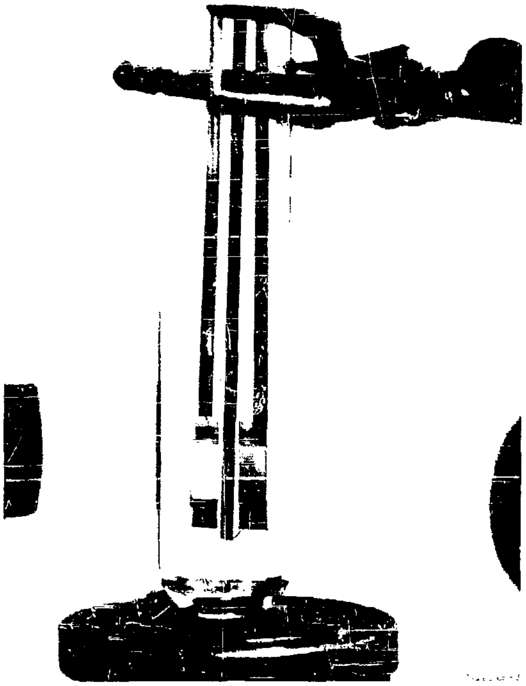


Figure 1 - Rhenium film resistor operating at 12 watts power

2.2 Dielectric Films

Progress on the search for high temperature dielectric films is illustrated in Fig. 2. As can be seen, several of the films, CeO_2 and Si_3N_4 are capable of going to approximately 450° C with less than 10% change in capacitance.(2) The search for higher temperature dielectrics is continuing. The ability to deposit and study the high temperature dielectric materials has been aided by a newly designed carbon crucible which is illustrated in Fig. 3. The crucible is arranged so that a liner of boron nitride may be used to contain the materials under study.(3)

The phenomena, reported in the last conference, of a sharp peak in the dielectric constant of zinc sulfide at a particular thickness, has been studied rather extensively.(4) A similar peak has been observed in SiO_2 films. It is believed that these anomalies are connected to the piezoelectric nature of the materials and is due to the stress on the films when they are deposited. The anomaly disappears if the films are annealed.

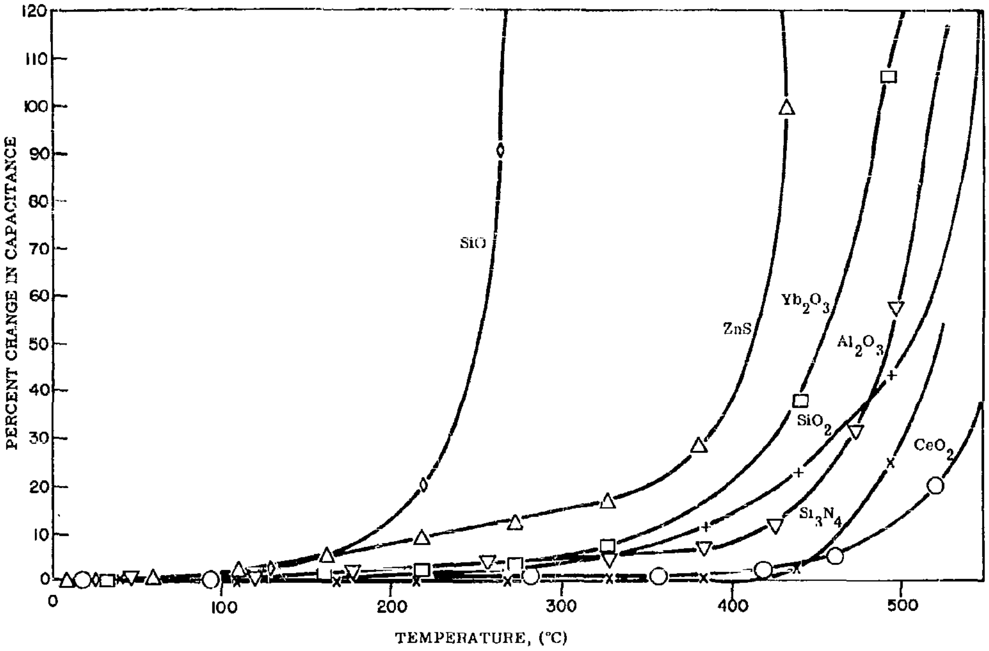


Figure 2 - Properties of dielectric films

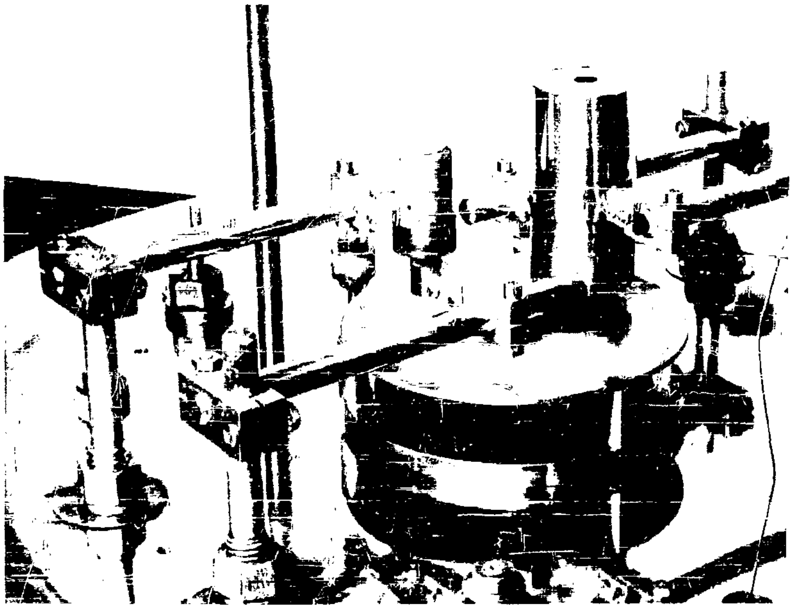


Figure 3 - High temperature deposition sources

2.3 Semiconductor Films

The mobility of vacuum deposited germanium films has been increased three fold since the last Navy conference. Films with mobilities as high as 600 cm^2/v-sec. have been formed at substrate temperatures of approximately 750° C. The increase in mobility has been brought about by the use of a substrate with an expansion coefficient similar to that of germanium. Silicon films formed by vacuum deposition to date have low mobilities; the highest mobility observed was 20 cm^2/v-sec. on film deposited at 1100° C. Some success has been achieved in sputtered films of intermetallic compounds such as InSb and GaAs. The sputtered films have the same conductivity type as the bulk material.(5) A mobility of 2400 cm^2/v-sec. has been obtained in InSb films. Studies on pyrolytically deposited silicon film has lead to the formation of large, pure, single crystallites which are useful for device formation.(6)

2.4 Active Deposited Devices

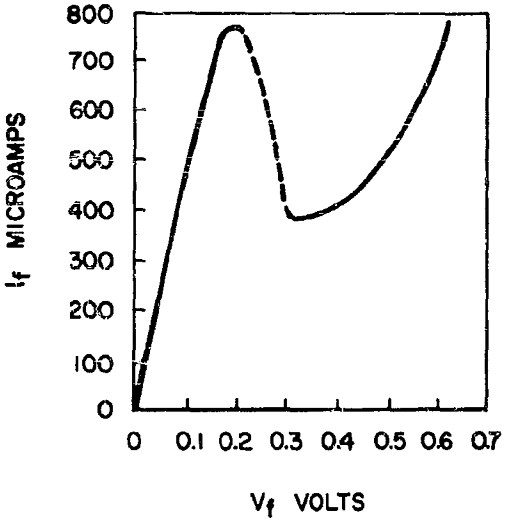
Increased emphasis is being placed on the formation of active devices. Two approaches have been taken. The first approach uses the properties of continuous thin films and interfacial effect and incompasses such phenomena as field effect, field emission and tunneling. The second approach uses the small single polycrystals formed in deposited films. Success has been had with both of these approaches. Field effect phenomena was discussed at the last Navy Microelectronics Conference and will be illustrated in the circuit described below. Studies of the effects in single crystallites have resulted in the formation of diodes and tunnel diodes. Figure 4, shows the manner in which tunnel diodes have been formed on silicon films deposited pyrolytically on fused silica substrates. The characteristics of such a device are shown in Fig. 5. The attachment of the leads was carried out by thermocompression bonding, however, some success has also been had with evaporated connections.

3. A FREQUENCY MODULATED PHASE-SHIFT OSCILLATOR

The studies on materials and effects are brought together in the fabrication of an electronic circuit. The circuit represents an exercise exemplifying the fundamental features of thin film circuitry. The use of distributed parameters, two dimensional shaping, and active circuit functions are all demonstrated. The resulting circuit lends verification to the predicted advantages to be gained in film circuits.

Figure 4 - Tunnel diode fabricated from pyrolytically grown crystallites

Figure 5 - Tunnel diode characteristic



The "heart" of the circuit is a distributed RC network in which the resistive element is a field-sensitive germanium film. The distributed component, which consist of a triple layer film, (germanium/silicon dioxide/gold) essentially uses surface and interfacial phenomena takes the place of 6 to 8 conventional components. The substitution of this single thin film functional device for a number of conventional components greatly increases the ultimate reliability that may be achieved.

4. CIRCUIT

The circuit is shown schematically in Fig. 6 and is composed of two functional blocks to establish the general criteria for oscillation. Assuming that the load is infinite, $GP_{in} = P_{in} + P_{loss}$ (where P = power) and the circuit will oscillate with increasing amplitude until this is satisfied by some limiting process. A second criterion is that the phase-shift around the loop must be zero, or the frequency will change so as to cause it to be zero. These conditions of unity power gain and zero phase-shift around the loop constitute Barkhausen's conditions for oscillation and lead to the following stability criteria: The best amplitude stability is at the point of greatest power gain vs. amplitude, and frequency stability results from large phase-shift with respect to frequency.

Figure 7 a and b gives the schematics of the distributed parameter circuit and its lumped constant counterpart.

4.1 Feedback Network

Given an amplifier, the feedback-modulator functional area must have the following characteristics.

(1) The phase shift must be such that the total shift around the oscillator loop is 0. Thus the network must provide 180°, 540°, etc., shift assuming a gain stage with an inherent 180° internal phase shift. Increased loss at the higher values of phase shift, however, prevents oscillation at any but 180°.

(2) The network should have minimum attenuation and sharp phase shift characteristics about 180° for good frequency stability.

(3) The phase shift must be continuously controllable to provide for frequency modulation.

(4) The feedback network should match the input and output impedances of the gain stage.

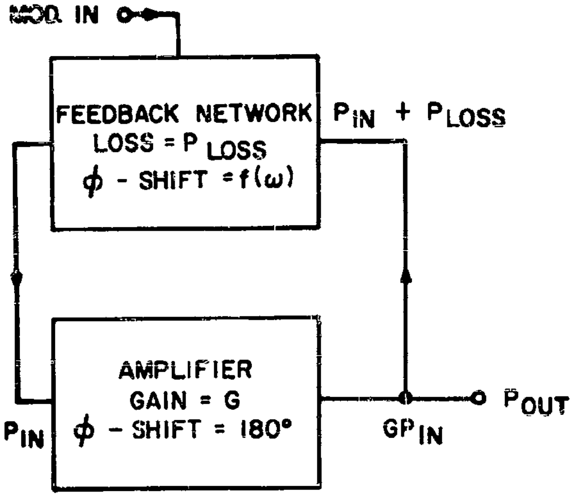
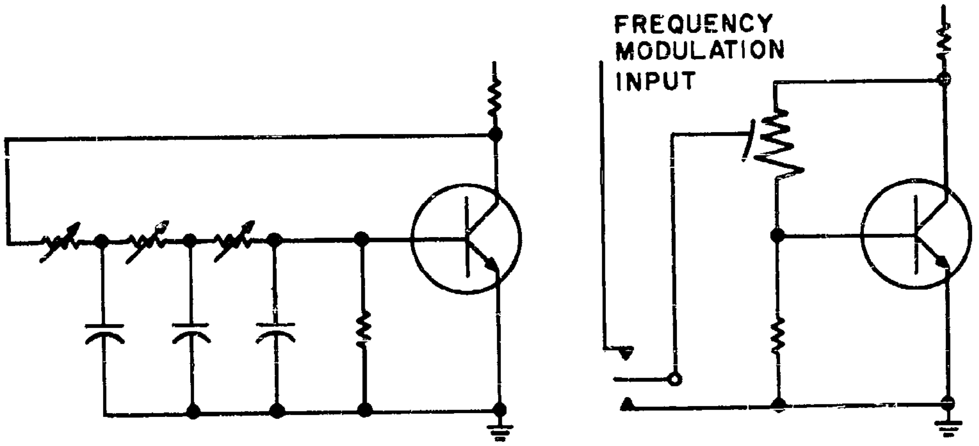

MOD. IN
FEEDBACK NETWORK
LOSS = P LOSS
ϕ - SHIFT = f(ω)
P_{IN} + P_{LOSS}
AMPLIFIER
GAIN = G
ϕ - SHIFT = 180°
P_{IN}
GP_{IN}
P_{OUT}

Figure 6 - Oscillator block diagram


FREQUENCY
MODULATION
INPUT

a. LUMPED CONSTANT b. DISTRIBUTED PARAMETER

Figure 7

The functions as outlined above may be met by the use of a three or four stage RC ladder with voltage sensitive capacitors or variable resistors to provide the modulation facility. These ladders of six or eight components having a phase shift of 60° or 45° per stage may also have a step impedance taper per stage. Consider the logical extension of this network to thin film technology: A continuous ladder line describable now in terms of capacitance and resistance per unit length of the form $C = Ce^{-2kx}$ and $r = Re^{2kx}$ where k is the taper parameter. This is accomplished by depositing a resistive film with an exponential geometry plus a capacitive field plate. The advantages of this configuration are:

(1) The phase shift vs. frequency characteristics have been improved, resulting in greater frequency stability.

(2) The network loss has been decreased by approximately a factor of three from a step tapered lumped constant circuit and a factor of 9 from an untapered lumped constant ladder.

(3) The network has an inherent impedance transfermation with an input-to-output impedance ration equal to the ratio of the initial and terminal resistive film widths.

(4) The entire feedback network now consists of only three vacuum deposited layers, thus greatly increasing the inherent reliability of the unit above the multi-element lumped constant counterpart.

If the resistive layer of the feedback network is deposited of a semiconductor material, this material will experience an enchancement or depletion of majority carriers when an electric field is applied and thus produce a change of resistance. This change is resistance, (field effect) in turn, produces a change in the phase shift of the network and the oscillator must seek a new operating point to satisfy Barkhausen's conditions, therefore producing frequency modulation as a function of phase shift network field plate potential.

4.2 Performance

Using a transistor as the amplifier element, complete FM oscillators have been operated in the range of several hundred kilocycles to over a megacycle. A typical unit, shown in Fig. 8, is described below.

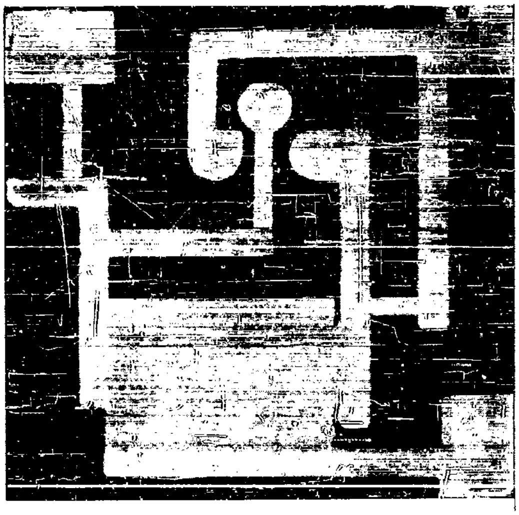
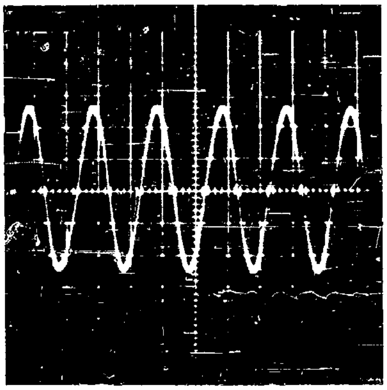
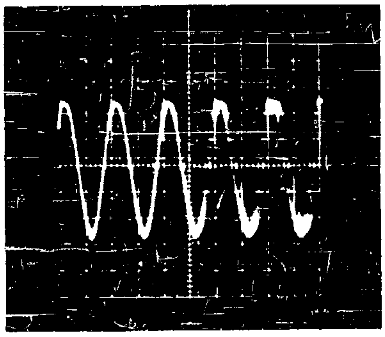


Figure 8 - FM oscillator



a. Unmodulated signal



b. Modulated signal

Figure 9

$R_1 = 7.2$ k

$R_2 = 2.9$ k

$R_3 = 10.0$ k

Transistor - 2N711

Figure 9 top shows the oscillator signal at 280 kilocycles sec.$^{-1}$ with no modulation. In the lower picture, the oscilliscope triggers at the same point while the frequency modulation causes a broadening of the trace with time. The picture shows 100 cycle modulation of 2.1 volts peak to peak, showing a modulation sensitivity of 1.18% modulation per volt or 3.3 kilocycles deviation per volt. Short range voice communication has been demonstrated with these units in conjunction with a microphone and receiver.

Although the circuit has been demonstrated using a conventional transistor as the gain element, the transmitter is primarily designed to accept a thin film field effect device. Due to the extremely high input impedance of these devices, the sign of the phase shift network taper may be reversed, resulting in considerably less network loss than in the case of the transistor.

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(1) Charles Feldman and H. E. Culver, Electronic Components Conference, May 2, 1961, San Francisco, California.

(2) C. Feldman and Michael Hacskaylo, Rev. Sci. Inst. 33 (1962) to be published.

(3) J. R. Piedmont and F. J. Hemmer, Rev. Sci. Inst. 33 (1962) to be published.

(4) Michael Hacskaylo and Charles Feldman, J. App. Phys. 33 (1962) to be published.

(5) C. W. Moulton, Nature 195, 793 (1962).

(6) E. G. Bylander and M. M. Mitchell 1962 AIME Semiconductor Materials Conference, August 27 - 29, 1962, Philadelphia, Pennsylvania.

INSULATED-GATE FIELD-EFFECT DEVICES FOR MICROELECTRONICS

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The class of transistors to be discussed here has a number of features that recommend it for individual devices, but its important distinction to us is that it may be the optimum choice for integration in a great many applications.[1] The electrical parameters of an idealized insulated-gate field-effect transistor are shown in Fig. 1. Some modifications of these parameters that might be dictated by various microelectronics applications are shown in Fig. 2. In an amplifier, elimination of any requirement for fixed gate bias may be convenient and a more linear characteristic may be desired. These modifications are incorporated in Fig. 2a. For logic circuits, a device that approximates a voltage-controlled relay is preferred. For reliable switching, the "on" and "off" control-gate voltages must lie well within the range of voltage available at the output (drain) electrode. Furthermore, the excursions of drain voltage should not introduce significant changes in impedance at the gate. These characteristics are illustrated in Fig. 2b. Note that similar characteristics are suitable for direct-coupled amplifiers without the need for voltage level-shift between stages. Other modifications that might be desired include scaling of impedance level as in Fig. 2c, or reversal of electrical polarities, as in Fig. 2d.

The physical principles that give rise to this versatility are illustrated in Figs. 3 and 4. In the first instance, the channel region between the source and drain is electrically neutral. Application of positive bias to the gate electrode causes electrons to enter the channel region; application of positive drain voltage gives rise to a lateral field that sweeps electrons out as fast as they enter. The mechanism for current saturation is similar to that for unipolar transistors: the net gate-to-channel bias becomes negative near the drain electrode and current becomes space-charge-limited rather than ohmic. The modifications implied by Fig. 2 are shown in Fig. 4. An initially n-type channel, Fig. 2a, must be depleted of mobile charge by a negative applied bias to cut off source-drain current. An initially p-type channel, Fig. 2b,[2] blocks current flow between n-type source and drain contacts; source-drain current flows only when sufficient positive bias has been applied to the gate, enhancing electrons, that the channel effectively becomes n-type (a similar situation may obtain due to the presence of traps). The voltage scale, and therefore the impedance level for transistors of equal lateral dimensions are directly dependent on the gate insulator thickness, providing the modification called for in Fig. 2c. Finally, complementary transistors employing hole conduction as in Fig. 4d provide for the characteristics illustrated in Fig. 2d.

Two very different fabrication techniques have been employed for insulated-gate field-effect transistors. Those made by a sequence of evaporations, including the evaporation of cadmium sulphide to form the channel regions, are called TFT's, for Thin Film Triode.[3] The major virtue of this approach is the freedom it offers in choice of materials and its suitability for making large arrays. We are working to establish compatibility of these techniques with those suitable for fabricating interconnections and passive thin film components and to insure the required reproducibility, uniformity and durability of the TFT's. This is being done in the context of two capabilities. One is directed toward digital correlation techniques,[4] which implies large arrays of similar TFT's with many interconnections, but a minimum of passive components. The other is typified by cockpit display requirements,[5] such as scanning, storage, waveshaping and amplifying functions, and requires a greater assortment of passive components and device characteristics.

The other major fabrication technique employed is based on silicon transistor technology. In this technology problems of uniformity, etc., are well under control, and our efforts are centered on improving device characteristics and establishing the validity of the concept we call "integrated logic nets."[6] This concept, in brief, is that most digital requirements will be satisfied most economically and reliably by integrated arrays of suitably connected "ideal switches." The "voltage-controlled relay" of Fig. 2b is our candidate for the ideal switch: the static characteristics illustrated permit series-parallel direct-coupled logic, and switching times (under ideal conditions of unity fan out) of the order of ten nanoseconds are observed. The topology and electrical symmetry of insulated-gate field-effect transistors simplify circuit interconnections. The circuit shown in Fig. 5a, for example, is integrated into the simple ladder structure of Fig. 5b. The circuit is basically a flip-flop with associated gates;[7] nine such circuits will be combined to form a resettable bi-quinary counter "deck," and five decks will be interconnected as a five-decade counter. This counter is to perform the function $f_2 = f/n$, where f is on the order of 30 megacycles, and n is selected to be one of 28,000 integers as prescribed by channel setting. We anticipate that integration of one entire deck per silicon "chip" will be feasible, based on projected yields. Integration of the quinary divider portion of the deck is now in process. Laminar ceramic packaging is employed; connections from the silicon chip to land areas on the package are made simultaneously by vacuum evaporation. Similar techniques have been employed in fabricating eight-neighbor logic modules under contract with Air Force Cambridge Research Laboratories, Office of Aerospace Research.[8] One such module is shown in the photograph of Fig. 6. The five decks of the frequency divider, in slightly different form will occupy a volume of about one-half inch cubed and dissipate less than two watts.

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1. The research reported here has been sponsored in part, by the Electronics Research Directorate of Air Force Cambridge Research Laboratories, Office of Aerospace Research, under Contracts AF19(604)-8040 and AF19(604)-8836.

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5. Nonr 3854(oo).

6. T. O. Stanley, "Integrated Logic Structures Employing Nets of Identical Elements," National Electronics Conference, October 10, 1960.

7. Nonr - 62-1084-d.

8. AF19(628)428.

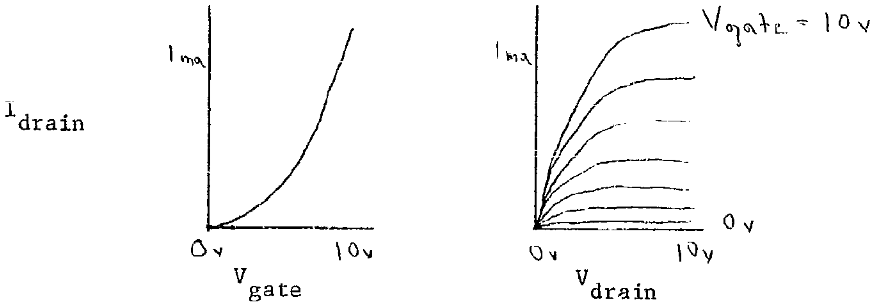

Fig. 1

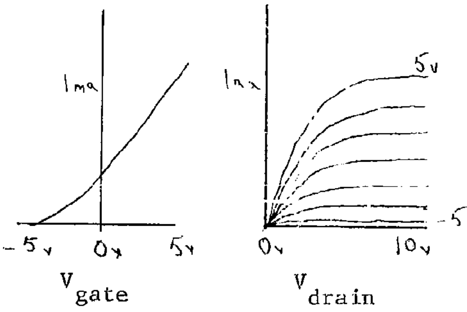

Fig. 2a

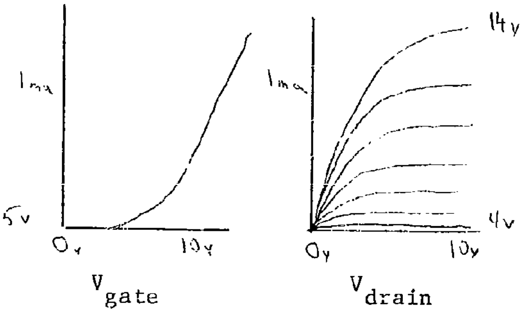

Fig. 2b

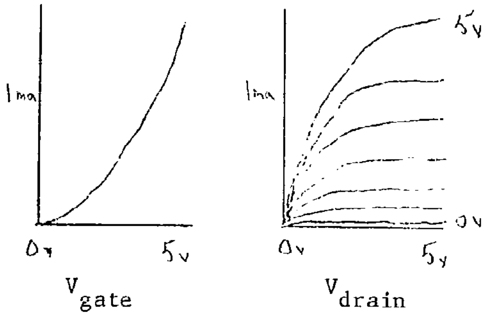

Fig. 2c

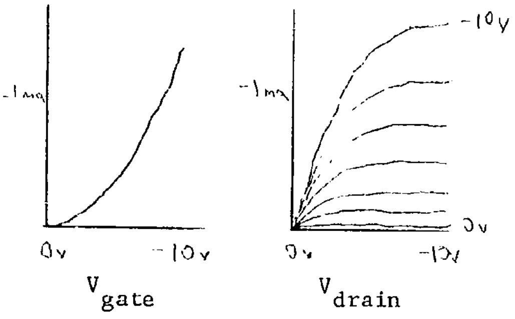

Fig. 2d

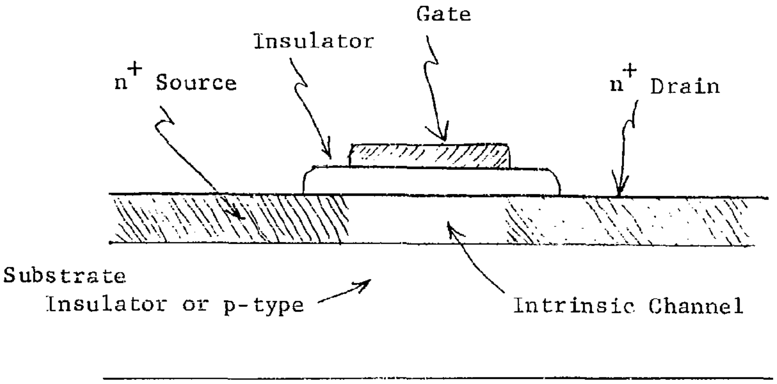
Gate
Insulator
n^+ Source
n^+ Drain
Substrate
Insulator or p-type
Intrinsic Channel

Fig. 3

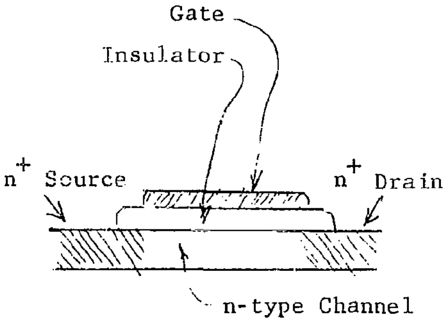
Gate
Insulator
n^+ Source
n^+ Drain
n-type Channel

Fig. 4a

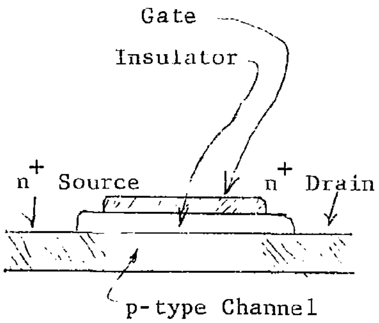
Gate
Insulator
n^+ Source
n^+ Drain
p-type Channel

Fig. 4b

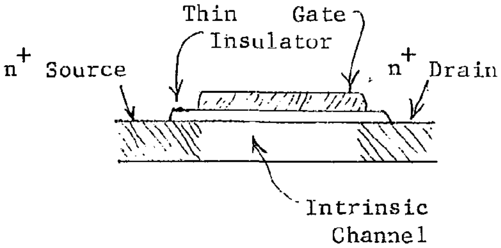
Thin
Gate
Insulator
n^+ Source
n^+ Drain
Intrinsic
Channel

Fig. 4c

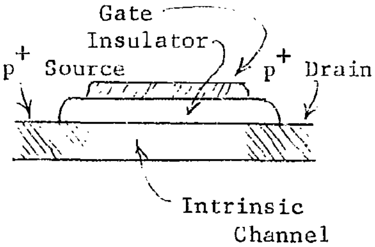
Gate
Insulator
p^+ Source
p^+ Drain
Intrinsic
Channel

Fig. 4d

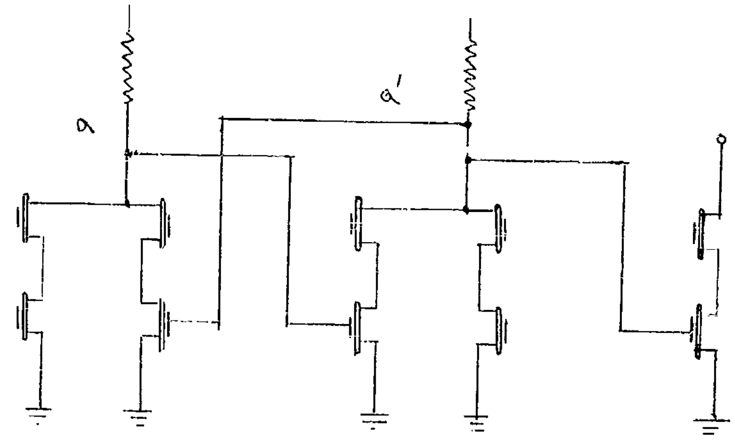

Fig. 5a

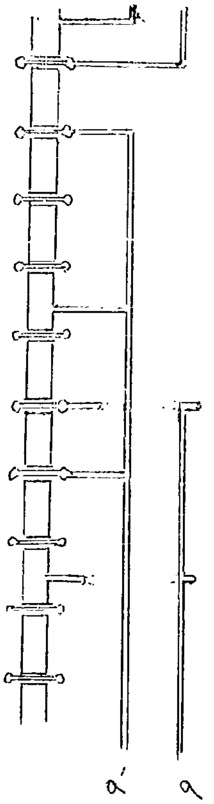

Fig. 5b

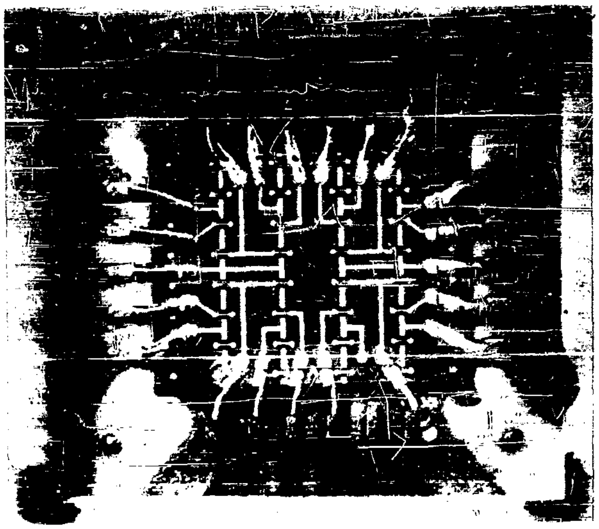

Fig. 6 Eight Neighbor Logic Modules

ADVANCED INTEGRATED PASSIVE AND ACTIVE THIN FILM TECHNOLOGY

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Sylvania Electric Products Inc.
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INTRODUCTION

In the period since late 1958, we have all observed the rapid emergence of a new field of technology called Microelectronics. In the early periods of growth, we witnessed the establishment of two radically different methods for forming microcircuits. Each would provide significant size reductions coupled with important cost savings over conventional electronic parts assemblies, and the avenue to a new breakthrough in electronic circuit reliability improvement. The two approaches referred to are the "silicon-based" or "diffused" and the "thin film" technologies. In the early days each approach was described as the answer to the increasing demands placed upon military electronic circuits and systems. With time and increasing understanding based on factual accomplishments, we can see a growing maturity in the Microelectronics industry, which is best exemplified by a growing realization of the fact that there is no single method of forming microcircuits which is best for all requirements. A mutual compatibility of silicon-based and thin film microelectronics has been well documented and demonstrated. Each satisfies some portion of the total electronic system and circuit spectrum of requirements best. Neither satisfies all the requirements best.

It is for this reason that Sylvania and other major corporations in the electronics industry are pursuing both avenues of attack in research, development and production with equal vigor.

OBJECTIVE OF THIS PAPER

This paper will concentrate on one aspect of Sylvania's Microelectronics activities: that of advanced thin film microcircuitry. Present status, present laboratory achievements, and future projections of technological growth will be indicated against the reference points of size and cost reduction versus calendar time.

A COMPLEX CIRCUIT AS A FRAME OF REFERENCE

An analog circuit in the form of an audio amplifier was selected as a frame of reference for illustrating where we stand in present day thin film microelectronics, what compromises we are forced to make to satisfy this circuit requirement on a reasonable basis, and to illustrate what will happen as a result of advanced research results now coming out of the laboratory. Figure 1 illustrates the details of the circuit and performance.

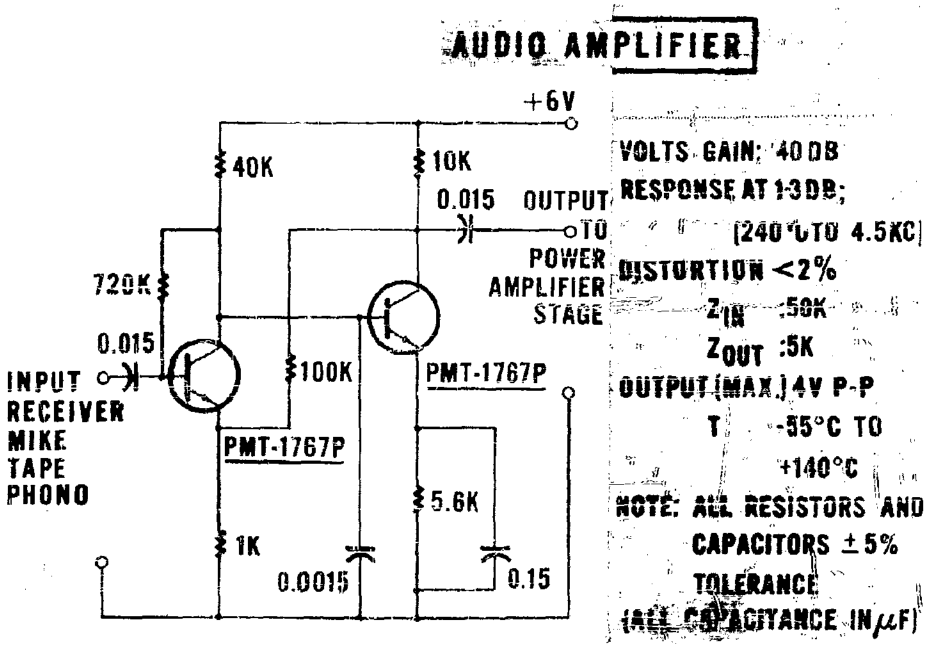
AUDIO AMPLIFIER
+6V
40K
10K
0.015
OUTPUT TO POWER AMPLIFIER STAGE
720K
0.015
INPUT
RECEIVER
MIKE
TAPE
PHONO
100K
PMT-1767P
PMT-1767P
1K
0.0015
5.6K
0.15
VOLTS GAIN: 40 DB
RESPONSE AT 1-3 DB;
(240 TO 4.5KC)
DISTORTION <2%
Z IN :50K
Z OUT :5K
OUTPUT (MAX.) 4V P-P
T -55°C TO +140°C
NOTE: ALL RESISTORS AND CAPACITORS ±5% TOLERANCE
(ALL CAPACITANCE IN μF)

Figure 1

Note that the circuit contains difficult requirements, in the form of high value circuit elements, and that performance standards have not been compromised to make the circuit easy to convert to microelectronics form.

Figure 2 is a scale layout of the audio amplifier circuit in thin film form, utilizing welded-in transistors. The most commonly used vacuum deposited dielectric material, silicon monoxide, (dielectric constant = 6) is illustrated. Resistors are vacuum deposited nichrome with the thinnest reliable film yielding 500 ohms/sq. The circuit conductor and resistor lines are vacuum deposited at 10 mils width. The dimensions of the thin film circuit are as shown in Figure 2. We do not propose that the audio amplifier be built in thin film form using these materials or techniques. To do so would be to follow an idealistic approach, at the expense of abnormally large size and the resultant high cost.

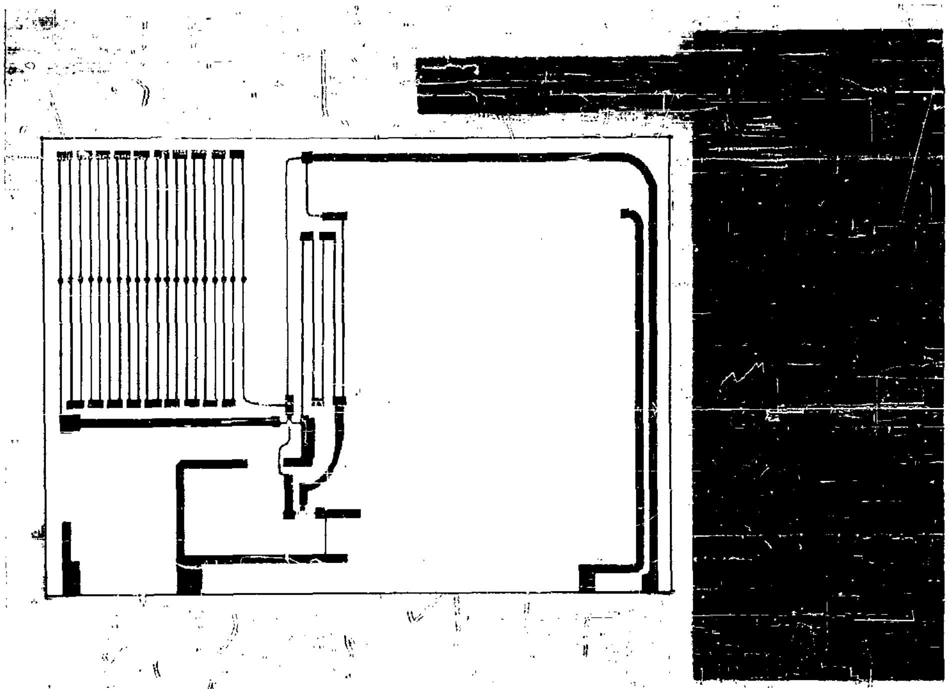

Figure 2

If we permit ourselves to compromise the current thin film technology, then we can observe several circuit elements whose large values are the major contributors to the excessive size of the audio amplifier in all thin film form as illustrated in Figure 2. Specifically we refer to the 0.15 mfd capacitor and the 720 K ohm resistor. If one accepts a compromise based upon the limitations of currently practiced thin film technology, then we can weld several individual components to the integrated thin film circuit and achieve a significant size reduction. Figure 3 is an illustration of the same circuit with the critically large circuit elements welded in place. Circuits of the size illustrated in Figure 3 (.35" x .8") can be built on Sylvania's Microelectronics Pilot Production Line in repetitive quantities right now. Costs are competitive with present day military quality, high density, individual parts circuit packaging techniques.

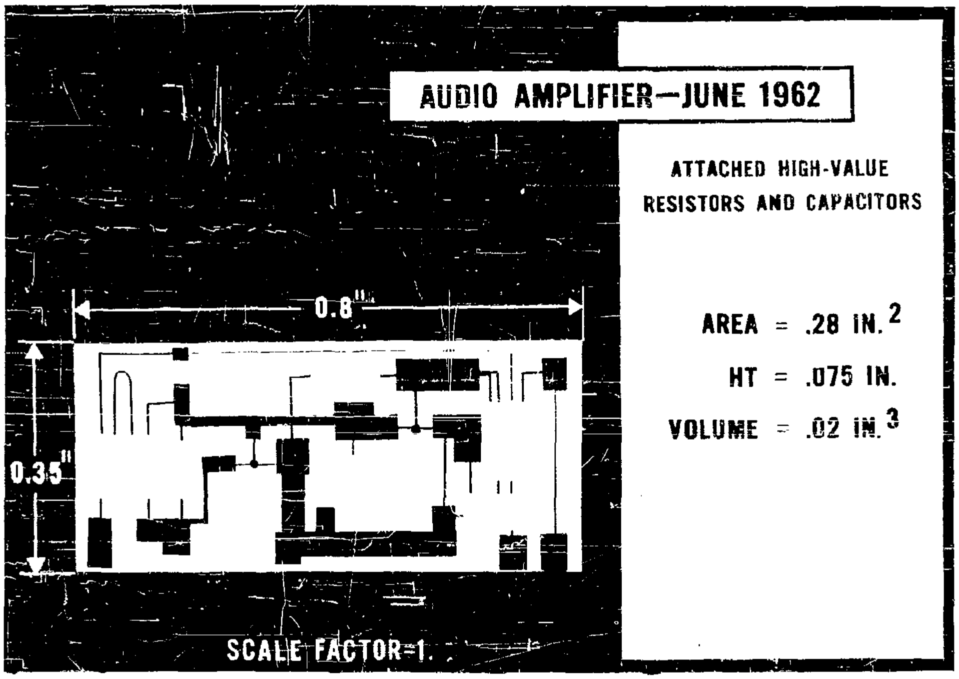
AUDIO AMPLIFIER—JUNE 1962
ATTACHED HIGH-VALUE RESISTORS AND CAPACITORS
AREA = .28 IN.^{2}
HT = .075 IN.
VOLUME = .02 IN.^{3}
0.8"
0.35"
SCALE FACTOR=1.

Figure 3

From the above illustrations it is apparent that if thin film microcircuitry is to progress and fulfill its growth potential, several technological improvements are necessary. First, we need thin film materials with dielectric constants which are significantly higher than 6, or even 25 which can be achieved from wet electrochemically anodized tantalum films. Sylvania has been developing the vacuum deposition of titanium dioxide (TiO_2) thin film capacitors in its laboratory for the past six months. These dielectric films are created by evaporating elemental titanium in a high vacuum system by heating a 1" diameter cylindrical slug of the metal with a projected high powered electron beam. (Beam power up to 20 KV and 300 MA). In conjunction with the electron beam evaporation of titanium, controlled partial pressures (10^{-3} to 10^{-5} mm Hg) of oxygen are maintained by oxygen injection during the evaporation process. This causes the evaporating titanium vapor to combine in transit, with the oxygen, and to arrive at the substrate surface as the titanium dioxide dielectric. Titanium or other metal electrodes can be formed by the simple stopping of oxygen injection. Such vacuum deposited thin film capacitors have been formed with capacitance ranges as high as 9 MFD per sq. in. with voltage breakdowns greater than 35, and in more conservative and reproducible fashion in the vicinity of 2 MFD per sq. in. with voltage breakdowns in the order of 70.

In addition, by controlling the oxygen injection rate during electron beam evaporation, it is possible to form partial metal oxides which are highly resistive. For example, the electron beam vacuum evaporation of aluminum in partial pressures of injected oxygen can be controlled to yield partial oxide aluminum-alumina films with resisitivities in the range of 5,000 ohms/sq. to 10,000 ohms/sq. Similar work on other resistive partial metal oxides is also being pursued. Present laboratory efforts are concentrating upon optimizing the process for 5,000 ohms/sq. resistive films. In addition, pure graphite has been evaporated with the projected electron beam to form carbon films in the 5,000 ohms/sq. range which exhibit performance characteristics very similar to the conventionally available pyrolytically decomposed and deposited carbon materials.

It should be noted that both processes (the formation of high dielectrics and highly resistive films) are completely compatible, since both use electron beam evaporation of basic and simple metals or carbon and achieve dielectric or resistive films by this simple control of injected oxygen.

Figure 4 is an illustration of the same audio amplifier laid out employing the TiO_2 dielectric constant 100 film, and the 5,000 ohms/sq. resistive film. One other factor has been added as part of the process improvement, and that is the development of electroformed metal masks for vacuum deposition with openings as narrow as .002", accurate to approximately 2%. By combining these technical accomplishments in one sequential series of process steps, it is possible to reduce the circuit size significantly as indicated in Figure 4.

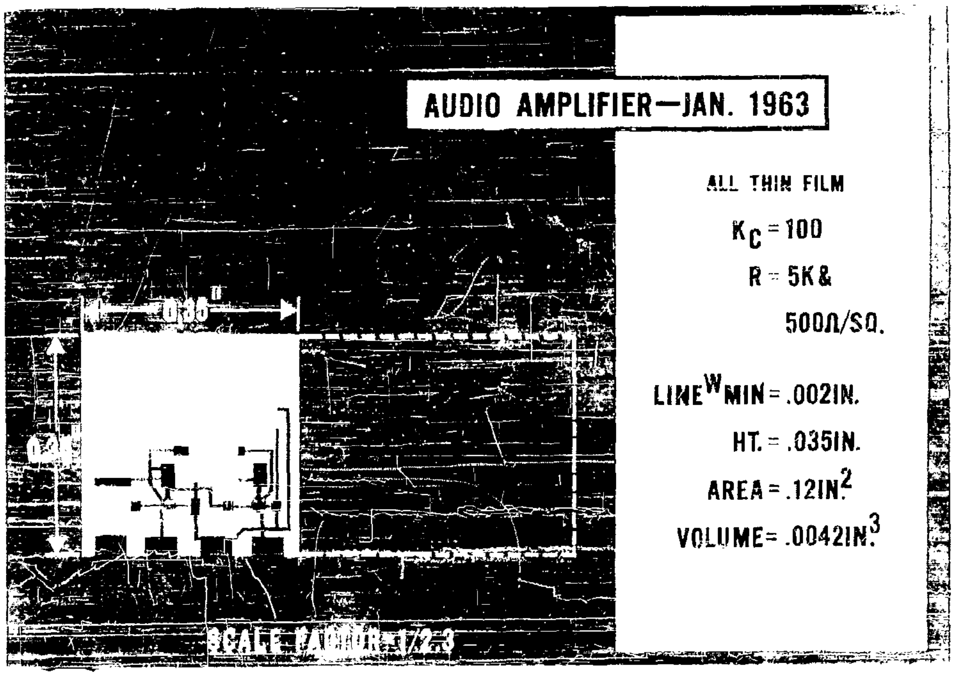
AUDIO AMPLIFIER—JAN. 1963
ALL THIN FILM
$K_C = 100$
R = 5K&
500Ω/SQ.
$LINE^W MIN$ = .002IN.
HT. = .035IN.
$AREA = .12IN^2$
$VOLUME = .0042IN^3$
0.36"
SCALE FACTOR 1/2.3

Figure 4

Reliable fine line width thin films require a substrate surface which is extremely smooth, inert, and free of sharp local discontinuities. Although glass microscope slides are in common use, our program studies have indicated that the poor thermal conductivity and thermal shock resistance of glass, coupled with its limited high processing temperature durability, make it only a temporary expedient material.

Ceramic substrates offer superior thermal and strength characteristics (ex. thermal conductivity over 30 times better than glass) but surface roughness forces the use of wider line widths and thicker thin films. An excellent combination would be a ceramic substrate with a very thin layer of high temperature glass on its surface. We are now completing the development of a high alumina (96-97%) substrate whose surface is coated with a special lead free glaze formulation which withstands thin film forming process temperatures of over 600°C. The glaze layer is in the order of .0005 inches thick, and is unaffected by thermal shock. Conventional leaded glaze layers of .002 to .003 inches thick impede heat removal, are more susceptable to thermal stress cracking, and interact with certain thin film materials.

A pilot production machine for electron beam and oxygen reaction vacuum deposited thin film formation of up to ten different sequential mask and material patterns on a controlled and repetitive semi-automated basis is presently under design at Sylvania, and is expected to be operational in the spring of 1963.

At this point it might be wise to break in on a description of the chain of technological improvements to call attention to one significant point. With improvement in thin film dielectrics and resistive materials and improvement in precision and fineness of line widths, it is now possible to produce quantities of thin film microcircuits in the space in which we previously could build only one. There are no extra process steps involved in building these additional circuits. Consequently one can expect significant cost reductions well below 50% of current military quality printed circuits, including an allowance for possible quantity induced yield reduction. (Note the scale factor in each of the figures.) The cost of attached active semiconductor devices must be added to the cost of each circuit.

Presently underway at other laboratories throughout the General Telephone & Electronics complex of which Sylvania is a part, is a research program aimed at achieving vacuum deposited thin films of high dielectric barium titanate (K = 1200) by oxygen-vapor combination. Preliminary results look encouraging, and this work, coupled with resistance films of 10,000 ohms/sq. as previously described, would yield the circuit sizes as illustrated in Figure 5.

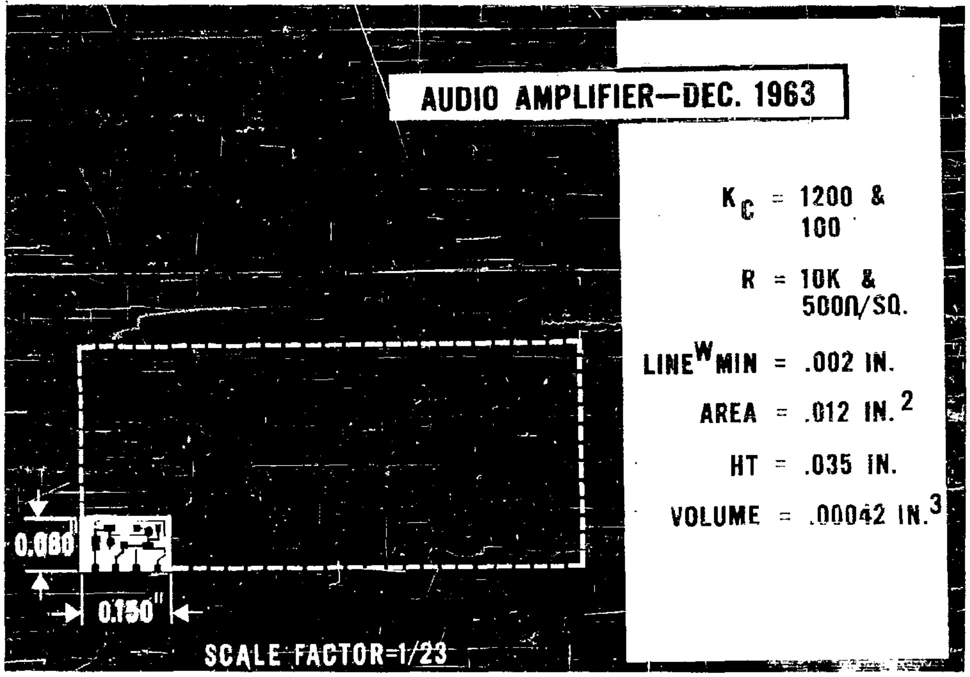
AUDIO AMPLIFIER—DEC. 1963
K_C = 1200 &
100
R = 10K &
500Ω/SQ.
$LINE^W MIN$ = .002 IN.
AREA = .012 IN.^{2}
HT = .035 IN.
VOLUME = .00042 IN.^{3}
0.080
0.150"
SCALE FACTOR=1/23

Figure 5

Up to this point in our technical discussion of the advantages of the improvements in thin film technology we have continued to use preselected and preprotected transistors attached to the thin film integrated circuit. Work underway at Sylvania's Microelectronics Laboratory at Waltham, Massachusetts has indicated and demonstrated that thin film silicon transistors and diodes can be formed on the same end-use substrate as the previously illustrated thin film passive networks. This is the long sought technical breakthrough that will permit us to form microcircuits in which each material does its job best in performing its portion of the total integrated circuit function. The ability to form thin film transistors and diodes directly from a vapor, terminated by thin film techniques, and married with thin film passive networks should yield the broadest range of microcircuit functions without performance compromise. Size reductions that will result from this breakthrough will be less significant than cost reduction and reliability improvement resulting from a decrease in the number of process steps necessary to form the finished optimized integrated thin film microcircuit. However, Figure 6 illustrates the additional small improvement in size that will be gained. Obviously, because so many more circuits can be formed on one substrate at one time using these techniques, significant cost reductions can also be anticipated.

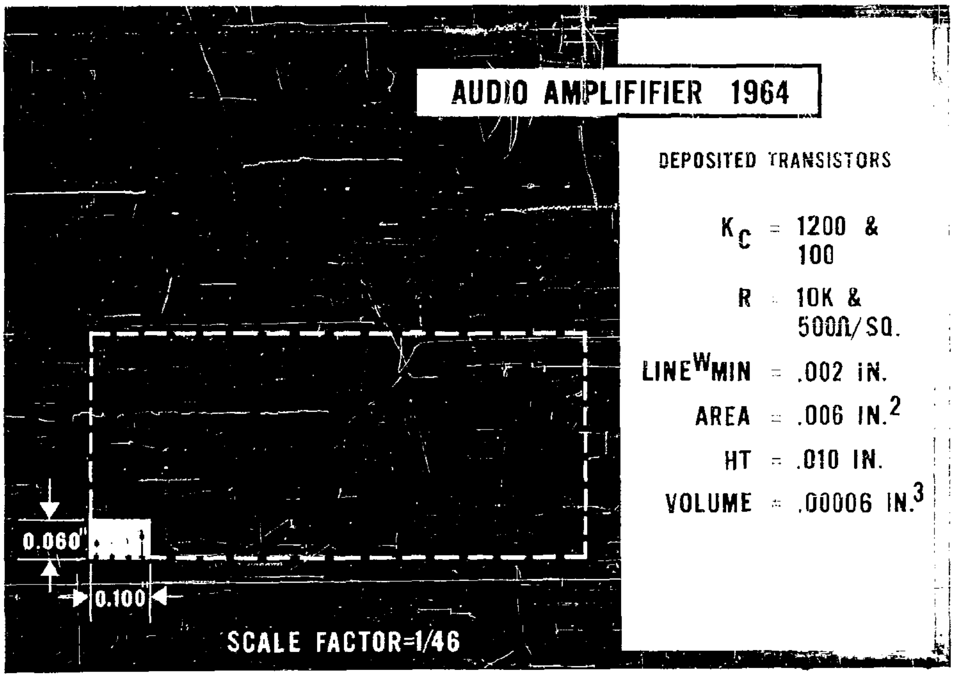
AUDIO AMPLIFIER 1964
DEPOSITED TRANSISTORS
K_C = 1200 & 100
R 10K & 500Ω/SQ.
LINE^{W}MIN = .002 IN.
AREA = .006 IN.^{2}
HT = .010 IN.
VOLUME = .00006 IN.^{3}
0.060"
0.100"
SCALE FACTOR=1/46

Figure 6

Although thin film silicon transistors and diodes are still under intensive research and development effort, some preliminary laboratory results may be of interest.

Figure 7 is a photograph of 9 silicon diodes, each with a .1" diameter junction area, formed directly from the vapor on a specially surface treated alumina ceramic substrate which is $\frac{1}{2}$" sq. The prior surface treatment of the alumina ceramic does not (and is not intended to) produce a single crystal surface on which the silicon film is grown from the vapor. The device quality silicon vapor growth takes place on this surface layer without benefit of surface layer crystal orientation or structure.

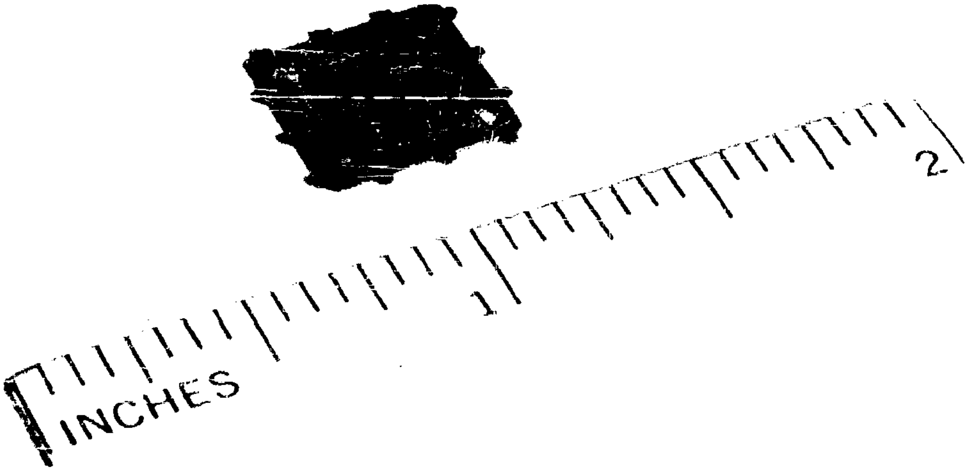

Figure 7

Diode characteristics measured on diodes such as those illustrated are shown in Figure 8.

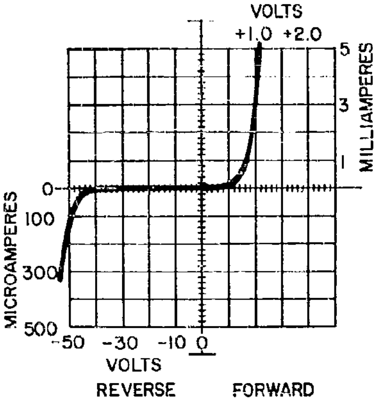

Figure 8

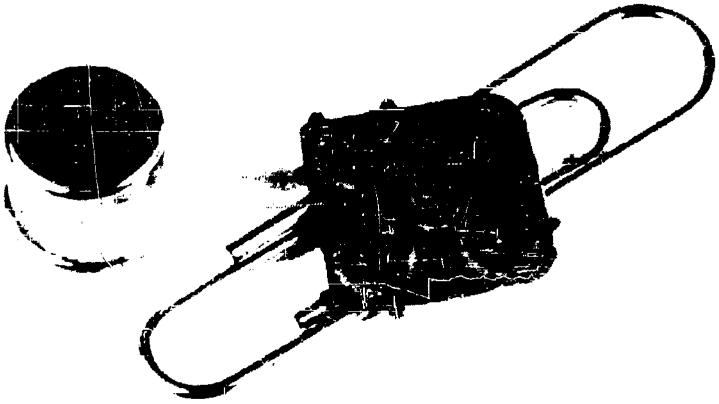

Figure 9

These results are on a laboratory research basis. Considerable improvement in device characteristics is anticipated with our continuing research effort.

Thin film silicon transistors have been formed using these same general techniques. Figure 9 shows five transistors, each with a junction area of approximately .1" in diameter, all formed from the vapor on this ceramic substrate.

Figure 10 is a photograph of the characteristics of these thin film transistors taken on a conventional commercial transistor curve tracer.

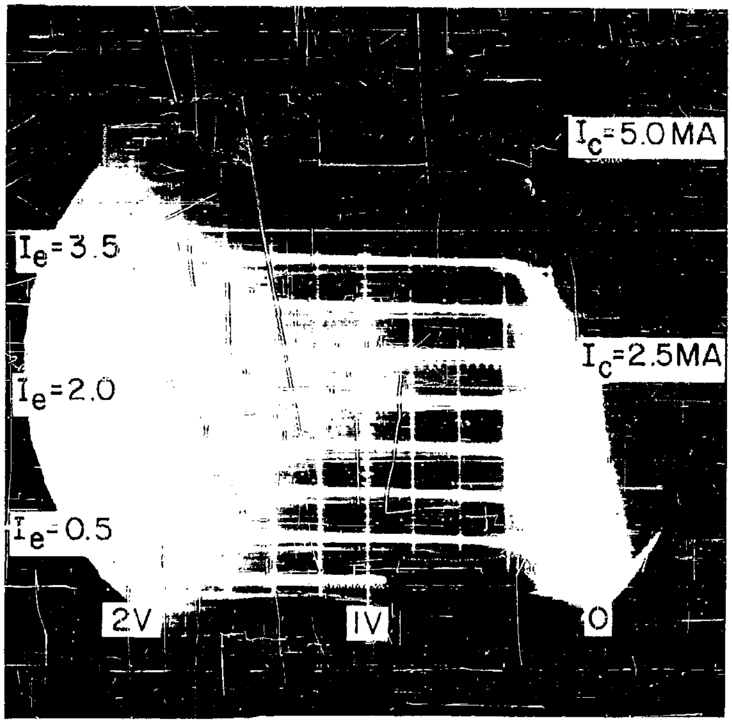

Figure 10

The above results on thin film silicon transistors and diodes are considered by Sylvania to be of preliminary and indicative nature only. Intensive continuing research and development efforts are underway to optimize the process and improve the resulting device characteristics. Current gain figures in the range of 20 to 200 have been measured recently.

CONCLUSION

This paper has attempted to show the many benefits that will accrue from the continuing improvement of thin film integrated microcircuit forming techniques and optimization of circuit-forming materials, using the Sylvania Microelectronics program and its results and outputs to date to illustrate the point, coupled with projections for the future.

The vacuum deposited integrated thin film approach to forming microelectronic circuits will be capable of forming the broadest conceivable range of semiconductor microcircuits without performance compromise. We wish to reiterate that there are many valid approaches toward the forming of microcircuits and that each will fill some portion of the system and circuit spectrum of requirements in an optimum manner. What portion of the range of microcircuit requirements the Sylvania thin film approach fills best will be answered by our proof and demonstration rather than by conjecture and prediction.

ACKNOWLEDGEMENTS

The work and developments described in this paper were funded by Sylvania Electric Products Inc., a subsidiary of General Telephone and Electronics Corp.; a number of patents are pending on these developments.

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SPECULATIVE RESEARCH IN MICROELECTRONICS AT STANFORD UNIVERSITY

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Stanford University
Stanford, California

To the present point, the most significant advances made in microelectronics can be classified as having technological origin. Procedures and processes made available through developments in the solid state field, primarily in the semiconductor field, have brought opportunity for making miniature counterparts of conventional systems through the integration of passive and active components.

In the advance which is apparent, the industrial laboratories, with their permanent staffs and specifically defined objectives, have produced the vast majority of new results. At the same time the desirability of a flux of novel and speculative ideas, with an expected lower fractional payoff, is a critical need for the extension of present results to new classes of capability. The university laboratory, with its Ph.D. candidates, a staff mostly of individuals rather than teams but always a temporary staff if the operation is successful, is adapted to undertake speculative projects for some of the same reasons that it is less adapted to take on the class of research with a technological base on which industry has been eminently successful. At Stanford University speculative projects related to microelectronics have been underway for about two years. This paper is devoted to a discussion of three of the Stanford projects.

Systems Which Are Operable Though Defective

In practically all microsystems the possibility of repair by replacement of individual parts is impossible. Yet it is virtually impossible to conceive large systems which have all parts working at the outset in manufacture and to continue to work throughout the system lifetime. Clearly, a new design strategy of systems is needed in which the system will continue to operate though certain of its parts are defective or deteriorate with life. It appears that systems which operate properly in spite of defective parts must have redundant elements. A suggestion for the use of redundancy in paralleled elements and a scheme of majority logic was made a number of years ago by von Neumann (1).

The basic idea underlying the use of redundancy is quite simple. One has a number of different elements or sub-systems in parallel working the same part of the problem. Their outputs are fed into a "vote-taker" which indicates the majority decision. It is clear that if there are three or more elements, the response of the majority will be correct, even in the presence of one defective channel.

The use of the combination of redundancy and adaption in which the nature or connection of a redundant system is changed in the course of life in response to the development of defects offers interesting possibilities. A form* of redundant system which utilizes adaption through application of an adjustable vote-taker has been proposed by Widrow and investigated by Pierce (2). The vote-taker in the system studied by Pierce can utilize different weights for the different channels in arriving at a decision. Figure 1 illustrates an adjustable vote-taker. The responses of paralleled parts supplying the input have +1 or -1 as the signal they supply to the vote-taker; these are their responses to the problem part they solve. The vote-taker multiplies the individual answers by the appropriate weight, sums the result and feeds this to a threshold element which gives +1 for any positive value and -1 for any negative value. One advantage of the adjustable vote-taker is that it can disconnect an incorrect channel by adjusting the corresponding weight to zero. A channel which gives opposite answers could be utilized by employing negative values for its adjustable weight.

The key to the use of an adjustable vote-taker is a procedure to arrive at values for the adjustable weights, an adaption procedure. Two methods of adjusting the vote-taker have been suggested by Widrow and Pierce. In the first of these, a system would be given test exercises where the correct answer of the stage being adjusted would be supplied separately. Channels agreeing with the correct result would have their vote decreased. The second method, attractive because of its simplicity, is based on the assumption that at the outset the majority of the channels feeding a vote-taker are correct. Channels which agree with the majority have their vote weights increased; those disagreeing with the majority have their vote weights decreased.

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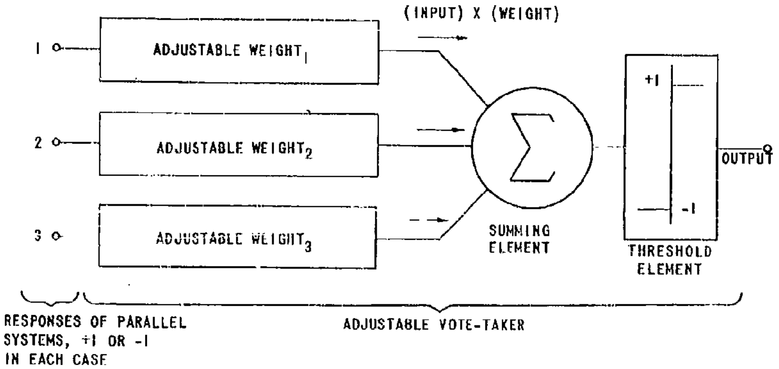
* Initial work on this research was carried out with support of the Joint Services under Office of Naval Research Contract Nonr 225(24).


(INPUT) X (WEIGHT)
1
2
3
ADJUSTABLE WEIGHT$_1$
ADJUSTABLE WEIGHT$_2$
ADJUSTABLE WEIGHT$_3$
SUMMING ELEMENT
+1
-1
THRESHOLD ELEMENT
OUTPUT
RESPONSES OF PARALLEL SYSTEMS, +1 OR -1 IN EACH CASE
ADJUSTABLE VOTE-TAKER

ADJUSTABLE VOTE-TAKER

Figure 1

Pierce has compared the probabilities of correct operation of three forms of a system made of 100 stages in which the probability of functioning properly of each stage is 0.9. One form is the system with no redundancy. The second form has redundancy and simple majority logic. The third form has redundancy with adaptive logic which are assumed to give correct answers requiring only one good channel. The probabilities of correct functioning of these arrangements for redundancies of 3 and 9 are as given below.

Probabilities of Correct Functioning of Systems of 100 Stages

No Redundancy	Redundancy 3 Major.	 Adapt.	Redundancy 9 Major.	 Adapt.
$2.7x10^{-5}$	.058	0.91	0.90	$(1-10^{-7})$

The implementation of adaption in redundant systems is in an early stage of development. At Stanford considerable research is going into the development of variable gain elements with memory, a necessary component in the adjustable vote-taker. In addition, the processes of adaption, the dynamics of the various forms of adaptive processes, and related forms of adaptive systems are being studied. In the course of time, this research and that directed along related lines in other centers can be expected to yield results of practical significance to future microsystems.

Design Theory of a Surface-Field-Effect Transistor

A characteristic of great importance for amplifiers in microsystems is their adaptability to integrated construction. One attractive form of amplifier for this function is the surface-field-effect transistor. The surface-field-effect transistor was discussed by M. M. Atalla at the Solid State Device Research Conference in June, 1960. At Stanford* a design theory for this form of device was developed by H.K.J. Ihantola under the supervision of J. L. Moll (3).

The form of surface-field-effect transistor discussed by Ihantola is shown in Fig. 2. The channel of the transistor is in the upper surface of the p material between the n regions which are diffused in to form the source and drain regions. The channel width is modulated by a signal to a gate electrode just as in the conventional field-effect transistor. In the surface-field-effect transistor the gate electrode is over an insulating region above the channel. In the form of structure discussed by Ihantola, the p material considered was silicon and the insulator was SiO_2. The thickness of the SiO_2 region was less than 1000 Angstroms. The gate region is a metal layer evaporated on the insulating region.

The performance of the surface-field-effect transistor can be understood qualitatively when one explains how a channel region of n conductivity can be caused to form between the source and drain by a gate voltage and be modulated in thickness by the gate voltage. For a zero gate voltage above the p region, the density of holes in the p region is essentially equal to the density of donor impurities in the p material. At the application of a

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* Research at Stanford on this project was under the support of the Electronic Technology Laboratory, Aeronautical Systems Division, United States Air Force, under Contract No. AF33(616)-7726.

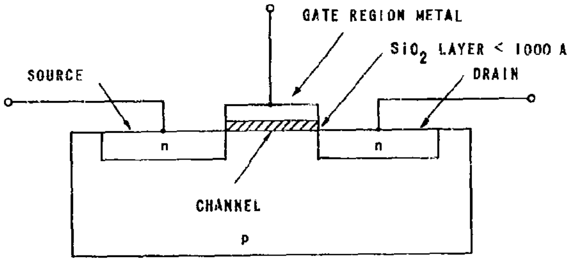


Figure 2 - SURFACE-FIELD-EFFECT TRANSISTOR

positive gate voltage, producing a field normal to the surface of the p material as illustrated in Fig. 3, the holes are forced away from the surface leaving there a region of high resistivity. At the application of a still higher gate voltage, the field is sufficiently high that electrons are drawn to the surface and a layer of material results, called an inversion layer, which is of n conductivity type. This situation is roughly described in Fig. 3, in which there are conduction electrons at the surface. Under them is a depletion region in which there are few carriers of any kind. Finally deep in the p material there is the usual conductivity character for p material, namely holes in density corresponding to the doping density. The critical feature of the surface-field-effect transistor is that the thickness of the inversion layer is modulated by the gate voltage, becoming thicker with increases in the gate potential with respect to the channel.

At this point the similarity of the surface-field-effect transistor to the conventional field-effect transistor is apparent. In the conventional field-effect transistor between the gate terminals there is a depletion region with a reverse-biased pn junction, the depletion region widening and the channel correspondingly narrowing as the gate junction is reverse biased further. In the surface-field-effect transistor the inversion layer is the channel and it is directly widened by the application of a positive gate potential. In both cases there is very small gate current. In the case of the surface-field-effect transistor the field is introduced through the thin insulating region and only minute currents flow for voltages below the breakdown value.

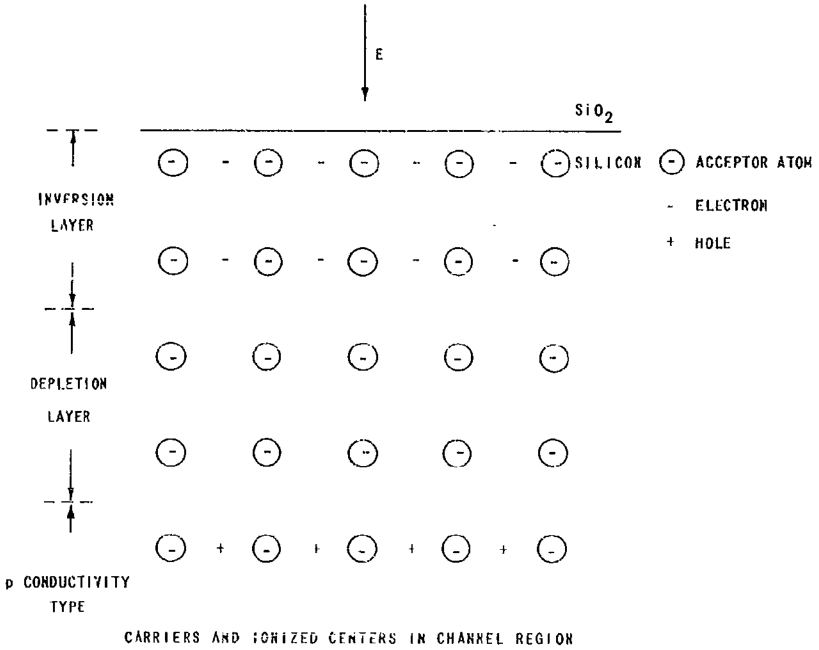
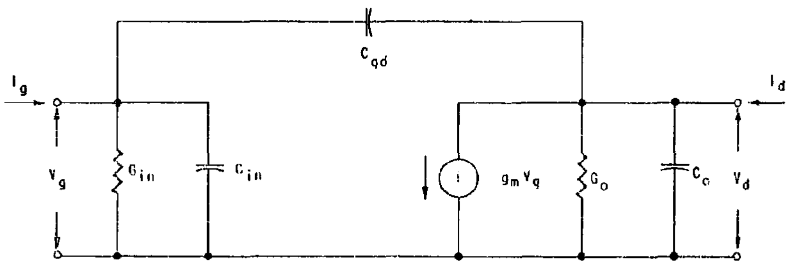

E
SiO$_2$
INVERSION LAYER
DEPLETION LAYER
p CONDUCTIVITY TYPE
SILICON
ACCEPTOR ATOM
ELECTRON
HOLE
CARRIERS AND IONIZED CENTERS IN CHANNEL REGION

Figure 3

At the flow of current from the source to the drain there is a voltage drop along the channel in both the conventional field-effect transistor and the surface-field-effect transistor. Consequently, the channel narrows as one moves toward the drain contact. In both types there is the pinch-off phenomenon and the transistor presents a very high incremental impedance when the current comes to the pinch-off value.

The design theory of the surface-field-effect transistor which Ihantola presents relates the properties of the physical structure to the elements of the circuit model shown in Fig. 4. He relates the channel thickness and conductivity to the gate voltage, obtaining quantitative relationships for the behavior described above. In particular he shows the procedure of selection of resistivity of the channel material, and dimensions of the channel, its length between the source and drain and the width (normal to Fig. 2.) The design theory which is applicable to the surface-field-effect transistor is roughly similar to that of the conventional field-effect transistor. Ihantola finds that structures with transconductances of a few



CIRCUIT MODEL OF THE SURFACE-FIELD-EFFECT TRANSISTOR

Figure 4

milliamperes per volt and cut-off frequencies of tens of megacycles appear practical in silicon.

A Superconductive Trapped Flux Memory

A little more than a year ago Deaver and Fairbank (4) reported in the Physical Review Letters experiments verifying the fact that a current-carrying superconductive loop has flux linking which must be quantized. Accordingly, the current in the superconductor itself can have only values which are integral multiples of the value corresponding to one quantum of trapped flux. Deaver and Fairbank confirmed that the quantum of flux corresponds to the theoretical value which is $2.07\text{x}10^{-15}$ webers. At Stanford D. J. Dumin, a graduate student working with J.F. Gibbons, successfully demonstrated recently a multi-level memory in which the levels exhibit quantum spacings*. Thus the memory involved exhibits the ultimate fineness of steps of a magnetic memory.

The superconductive coil which traps flux in its axis is illustrated in Fig. 5. The structure consists of a sheet of lead, with which the coil will be identified as seen presently. On the lead is deposited a small strip of SiO, 1 mil wide and about 1000 A thick. The SiO strip becomes the axis (or hole) of the superconductive coil. Over the strip is deposited a bridge-like structure in lead,

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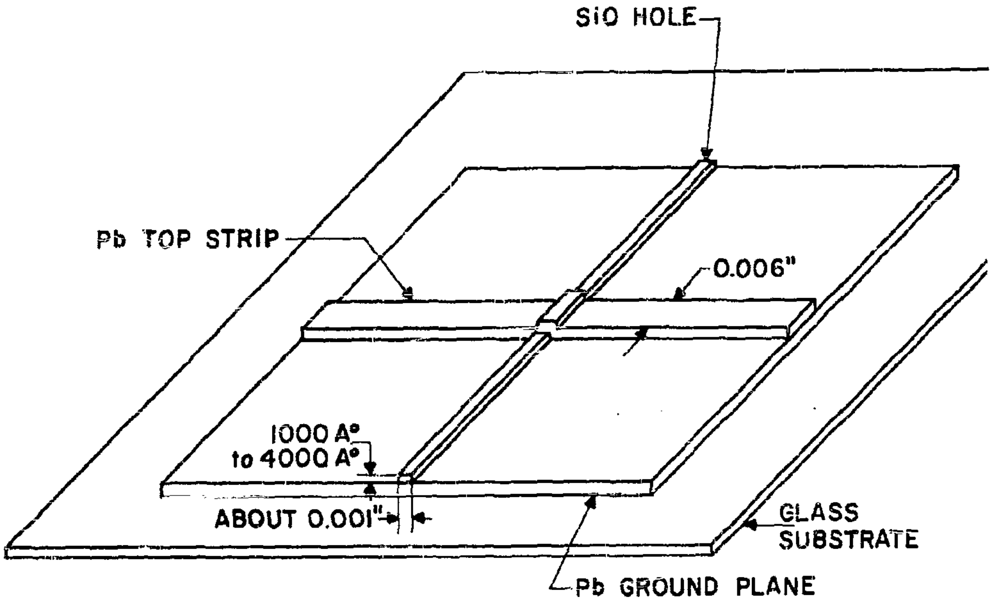
* Research at Stanford on this project was under the support of the Electronic Technology Laboratory, Aeronautical Systems Division, United States Air Force, under Contract No. AF33(616)-7726.

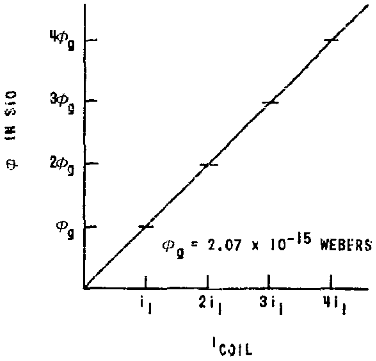


ARRANGEMENT OF SUPERCONDUCTIVE MATERIAL FOR TRAPPED FLUX MEMORY

Figure 5

as shown in the figure. The bridge of lead comes in contact with the lead sheet on both sides of the strip. The superconductive coil is identified with the bridge and plate combination which surrounds the SiO strip. One finds that each quantum of flux for the inner cross section dimension of the coil, 1 mil by 1000 A, corresponds to a field strength of 8.2 gauss.

The trapping of flux in the SiO hole of the coil is brought about in the following way. A much larger exciting coil, not illustrated in Fig. 5, but coaxial with the SiO strip, is used to set up a field in the SiO strip during a time when the lead is at a temperature above its critical temperature and is accordingly not superconducting. The relationship between flux threading the lead coil and current in the external exciting coil is shown in Fig. 6. On the straight-line are shown integral multiples of the quantum values of flux. First one places a fixed value of current in the external coil and reduces the temperature

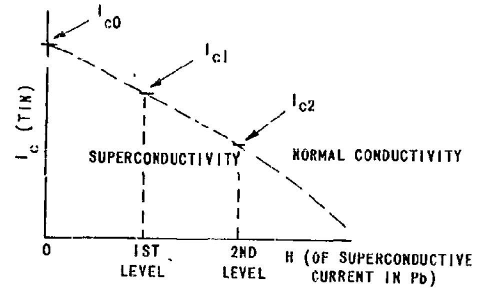


FLUX IN SiO VERSUS EXTERNAL COIL CURRENT
FOR LEAD NOT SUPERCONDUCTUVE

Figure 6

of the lead below the critical value which makes it superconductive. He then decreases the current in the external coil to zero, finding that a superconductive current is set up which keeps an integral multiple of the quantum levels of flux going through the SiO. If the coil current is closest to i_1 the trapped flux is ϕ_q, if the current is closest to $2i_1$ the trapped flux is $2\phi_q$, and so on. Moreover, the flux persists in the SiO indefinitely, so long as the lead remains superconducting.

Dumin has utilized an interesting means to sense the value of the flux trapped by the superconductive current in the lead coil. The flux threading the coil goes under the bridge through the SiO and then closes back on itself through space. There is a field strength in the region just above the lead bridge which is quantized in correspondence to the quantized flux. Dumin has measured the value of field here in a way which constitutes a nondestructive readout of the number of quanta of trapped flux. He does this by placing a strip of tin, isolated by a SiO layer, over the lead bridge. The tin is the detector of the quantized flux as we now shall see. The tin is in the field of the quantized superconductive current. Tin itself is a superconductor, but only for sufficiently small values of current and field. The regions in the current-field strength plane corresponding to superconductivity and normal conductivity are shown in Fig. 7. The tin becomes resistive for zero superconducting current in the lead at a



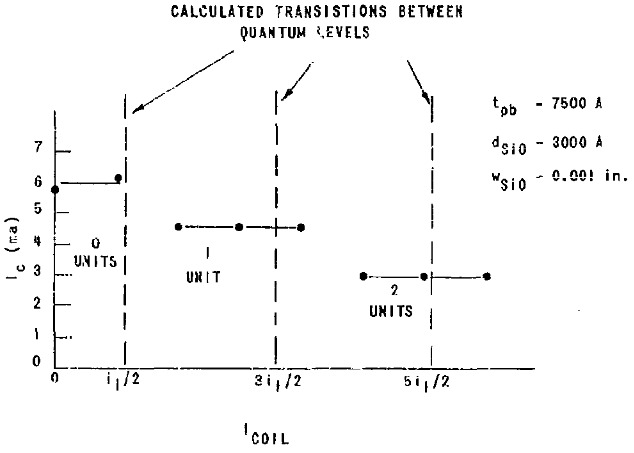
CRITICAL VALUES OF CURRENT IN TIN DETECTOR FOR
A RANGE OF MAGNETIC FIELD STRENGTHS

Figure 7

value of tin current I_{co}. When the lead carries a superconducting current corresponding to the first quantum of trapped flux, the tin detector becomes resistive at I_{c1}, a value of current less than I_{co}. For a sequence of higher quantum levels of trapped flux, the critical detector currents are a sequence of lower values as illustrated in the figure.

In Fig. 8 are shown experimental data on a particular device having the lead ground plane and bridge of thickness 7500A, the SiO strip of thickness 3000A and width .001 in. A sequence of values of current in the external coil were applied, the lead was made superconductive and the coil current shut off. Finally, the critical current in the tin detector was measured. The dashed vertical lines show computed values of coil current corresponding to $i_1/2$, $3/2\ i_1$ and $5/2\ i_1$, of Fig. 7. These values would be expected to be the boundaries between the sequence of quantum levels of trapped flux. They are in approximate agreement with the range of the test points observed which illustrate three levels with precision.

At this stage Dumin has demonstrated possibility of superconductive trapped flux memories having levels of the ultimate fineness. The question of practical utility of the phenomena in practical cases must await further study for an answer.



MEASURED CRITICAL CURRENTS IN TIN DETECTOR FOR A SEQUENCE OF EIGHT VALUES OF CURRENT IN EXTERNAL COIL

Figure 8

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RELIABILITY REQUIREMENTS IN MICROELECTRONIC SYSTEMS

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General Electric Company
Syracuse, New York

1.0 Introduction

The essential need for electronic equipment and systems which can perform reliably and with minimum maintenance over a given time period has become one of the most important considerations facing manufacturers and users of electronic systems. Microelectronics has raised the hope that significant increases in reliability can be obtained by virtue of reduction of interconnections and by greater control of materials and processes in fabricating many circuit elements on a single substrate within a single manufacturing cycle. In addition, it is hoped that the size, weight and cost reductions which may be made possible by mass producing integrated circuits will allow economical introduction of redundancy on a component and circuit level. It is the intent of this paper to discuss in some detail the factors which influence reliability and relate these factors to microelectronics.

2.0 Reliability Factors

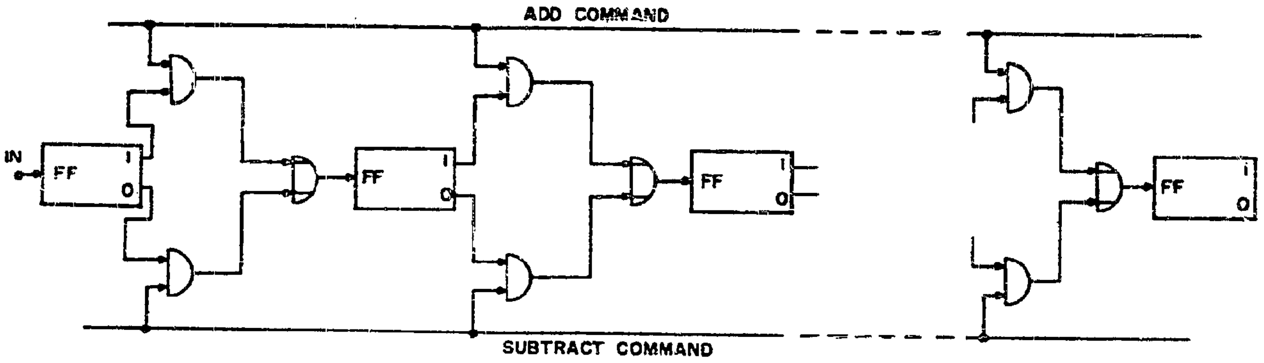
Reliability must be considered on a combined component, circuit and system level. Some of the factors which influence component reliability are operating temperature, electrical stress, thermal conductivity, immunity from contamination, stability of interfaces obtained when interconnection is made to other components and mechanical strength. However, circuit and system design is as critical to reliability as component quality. In general, the circuit and system designer can do little to improve the quality of the components he has to work with, but he can do a great deal to optimize the way components are used and thus insure maximum reliability within the limits set by the components themselves.

A principal factor in circuit and system design is simplicity. The less complex a circuit or system is made in order to perform a particular job, the more reliable it generally will be. Another important factor affecting reliability is cost. The old adage, "you get what you pay for", is old because it is true. In general, reliability will have to be paid for in the form of more quality control, more engineering design and possibly less standardization. Some of these factors will be considered below in more detail relative to specific system applications. In view of the general complexity of the subject of reliability, only simple logic circuits will be used to illustrate the points.

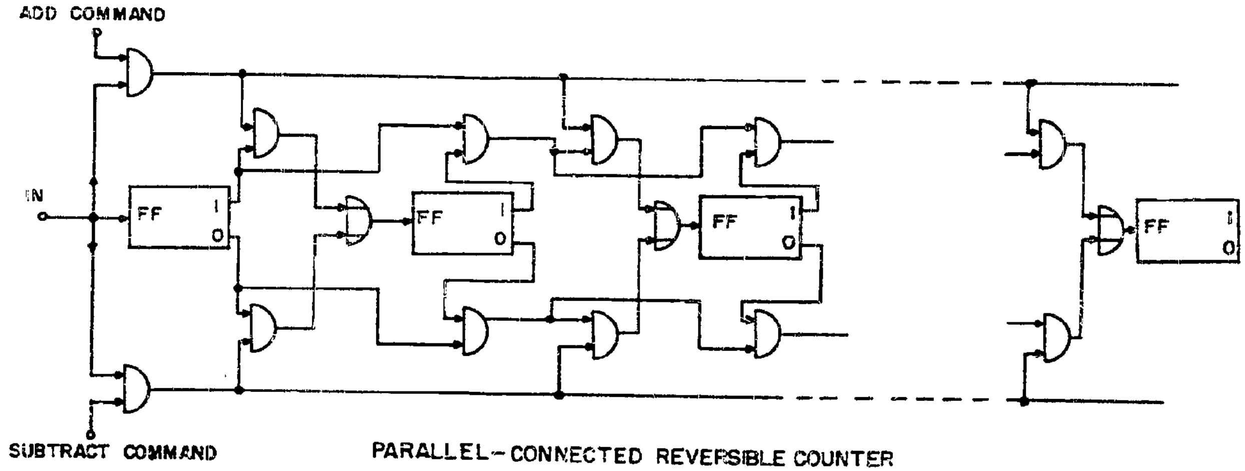
2.1 Circuit Complexity

Circuit complexity may be regarded as the number of components required to perform a specific function in a system. Microelectronics complicates the definition because of the ambiguity of the word "component". In the conventional sense, a circuit comprising three resistors and two transistors would be thought of as having five components. However, if the resistors and transistors are fabricated on a single semiconductor substrate with no external interconnections required between them, does the entire array now constitute a single component? For purposes of this discussion, it will be assumed that the number of interconnections required to utilize components in a particular function is a measure of the "complexity" of the circuit or system. This measure gives microelectronic devices a significant edge over conventional components, but it is precisely this advantage that leads to the hope that microelectronic technology will greatly improve reliability. Only experience based upon many hours of microelectronic system operation, compared to discrete-component system operation, can ever verify the correctness of this assumption.

One of the important ingredients of simplicity, particularly in digital systems is speed. If functions can be performed serially instead of in parallel, considerable advantage may be gained in reducing the complexity of the over-all system. Thus, an important criterion in evaluating microcircuits is the determination of their speed capabilities. For example, Figure 1 illustrates a reversible counter which in one case is serially connected and in the other, parallel connected. It is obvious that the parallel connected counter is considerably more complex than the serial configuration. However, it is necessary to use a


ADD COMMAND
IN
FF
1
0
FF
1
0
FF
1
0
FF
1
0
SUBTRACT COMMAND

SERIALLY-CONNECTED REVERSIBLE COUNTER


ADD COMMAND
IN
FF
1
0
FF
1
0
FF
1
0
FF
1
0
SUBTRACT COMMAND

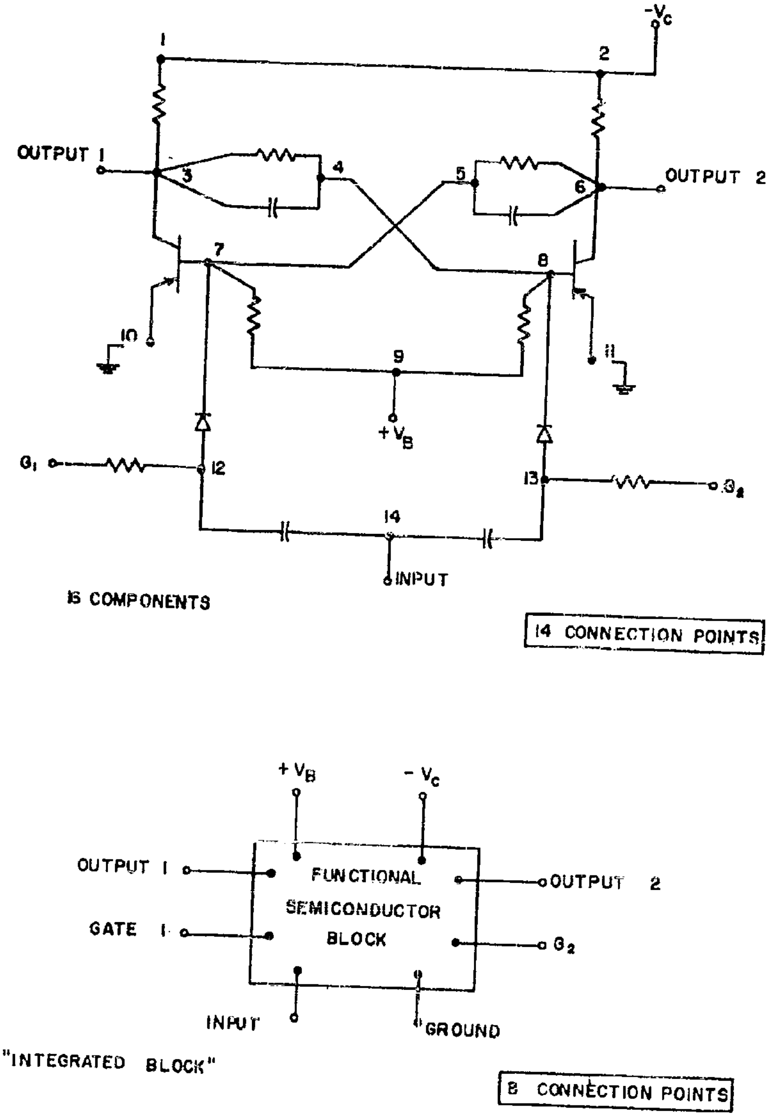
PARALLEL-CONNECTED REVERSIBLE COUNTER

FIGURE 1

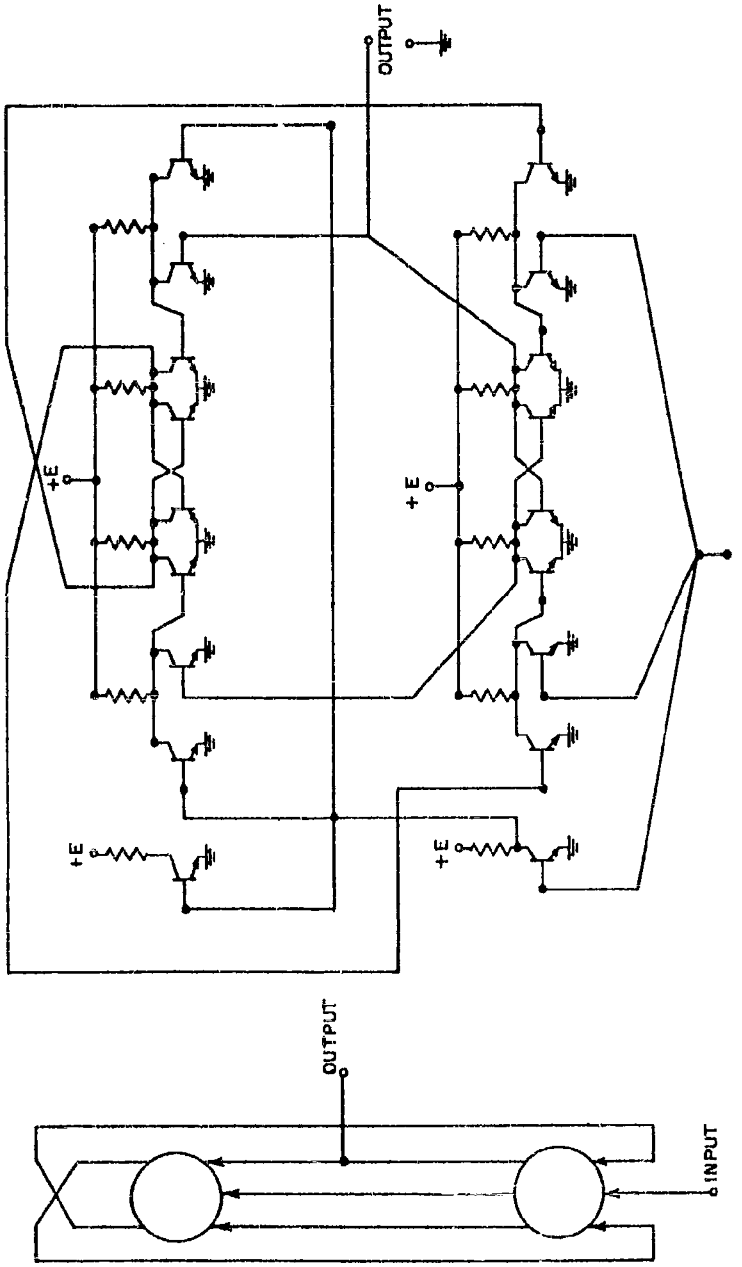
parallel circuit if the flip-flops do not have high enough speed to allow for the signal to propagate through the length of the counter between add and subtract pulses. If conventional discrete-component flip-flops and diode gates are used to realize a 10-stage reversible counter, 295 discrete nodal connections would be required in the serial configuration, counting the connections as shown at the top of Figure 2. For simplicity, each node is considered a single connection although several physical connections may be required to establish the node. However, the number of nodes goes up to 344 if the parallel configuration must be used. This represents an increase in complexity of almost 20%, a penalty which is exacted because the circuits are not fast enough. Now if integrated functional components are used to perform the same reversible counting function, and it is assumed that each flip-flop and each logic gate can be fabricated in integrated form and counted as a single component, the number of nodes required in the serial reversible counter would be reduced from 259 to 228, counting the connections as shown at the bottom of Figure 2. Similarly, for the parallel configuration, the number of nodes would be reduced from 344 to 308. In either case, it is seen that the integrated circuit approach results in a fairly sizable decrease in complexity as measured by the number of nodes. However, it is also of interest to note that if the functional component imposes a speed penalty, which in turn necessitates the use of a parallel configuration instead of a serial configuration, then no reduction in complexity would be realized with microcircuits compared to the counter made with discrete components having higher speed capability.

Another important consideration relating to system complexity concerns the trade-offs which have to be made between circuit design and device simplicity. From a microelectronic fabrication point of view, it would be most desirable to hold the numbers of types of components required to an absolute minimum. Thus, from a device point of view direct-coupled transistor-logic (DCTL) or resistor-transistor logic (RTL) would be considerably more desirable than integrated circuits using diodes and capacitors in addition to resistors and transistors. It may also be argued that, from a device point of view, reliability in such simple modules would be considerably greater than modules requiring more types of components since the number of fabricating steps and processes might be fewer.

However, the exclusion of certain components, such as capacitors and diodes, may be expected to result in an increase in complexity on a system level for some types of applications. For example, compare the DCTL center point triggered flip-flop shown in Figure 3 to the conventional flip-flop shown in Figure 2. In order to build a 10-stage serial counter with the DCTL flip-flop, 500 nodes


-V_C
1
2
OUTPUT 1
3
4
5
6
OUTPUT 2
7
8
10
9
11
+V_B
G_1
12
13
G_2
14
INPUT
15 COMPONENTS
14 CONNECTION POINTS
+V_B
-V_C
OUTPUT 1
FUNCTIONAL
SEMICONDUCTOR
BLOCK
OUTPUT 2
GATE 1
G_2
INPUT
GROUND
"INTEGRATED BLOCK"
8 CONNECTION POINTS

FLIP-FLOP AND PULSE TRANSMISSION GATE
FIGURE 2


OUTPUT
+E
+E
+E
+E
INPUT
OUTPUT
INPUT

D.C.T.L. TRIGGERED FLIP-FLOP-(SERIAL COUNTER STAGE)

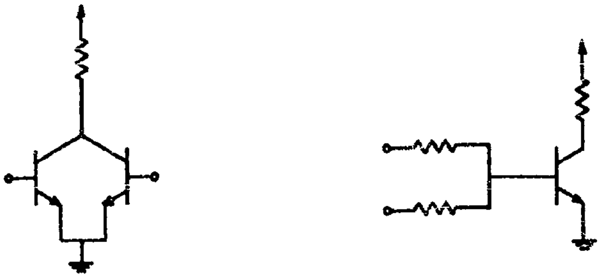
FIGURE 3

would be required as opposed to 160 for the conventional Eccles-Jordan configuration. Now if the entire flip-flop of Figure 3 could be considered as a single component fabricated in functional form, the total number of nodes for the 10-stage binary counter would be reduced from 500 to 170, a very sizable decrease in system complexity. However, note that the conventional counter employing discrete components is still less complex than the binary counter employing functional blocks. It should be emphasized that this disadvantage occurs only in sequential logic circuits, but in some digital systems these comprise as much as 25 to 75% of the entire system complexity. In systems where parallel logic nets dominate the design, the disadvantage of DCTL or RTL would be eliminated. But the point is that complexity should not be enhanced on the component level, only to be degraded on the system level, or vice versa.

3.0 Standardization

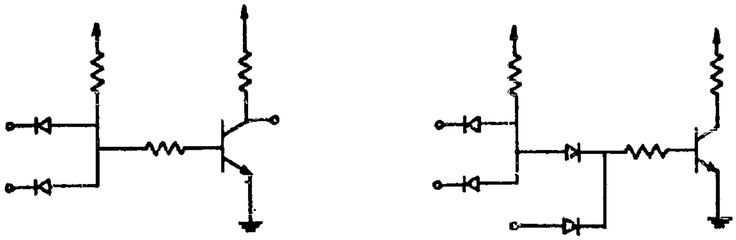
Standardization is particularly important to reliability because it minimizes the different number of parts that have to be made, consequently reducing fabricating processing steps and also reducing the inventory problem associated with equipment maintenance. In addition, standardization should result in lower costs due to the greater volume of similar circuits which can be produced.

However, from a system point of view, overstandardization can result in reduced reliability. As a first step in standardization, specific circuit configurations must be selected and others excluded for performing particular circuit functions. Figure 4 illustrates six possible configurations which may be involved. The selection of a particular configuration may depend upon the validity of past experience when extrapolated to microelectronics. For example, the DTL NOR circuit shown in Figure 3 involves more single components, such as diodes and resistors, to perform a given function than the DCTL configuration. However, the pre-microelectronic considerations which generally dictate the choice of DTL over DCTL were based upon the assumption that the transistor was the weakest link in the system, from a reliability point of view, and that diodes and resistors were necessary in order to provide greater isolation, greater immunity to noise and more effective bias stability. Thus, passive components, such as resistors, were used to establish threshold and signal levels while the transistor itself was called upon only for gain. In DCTL, the transistor properties themselves determine bias stability, threshold levels and signal waveforms. If the DTL circuit is fabricated on a single semiconductor substrate, there is no reason to expect that the



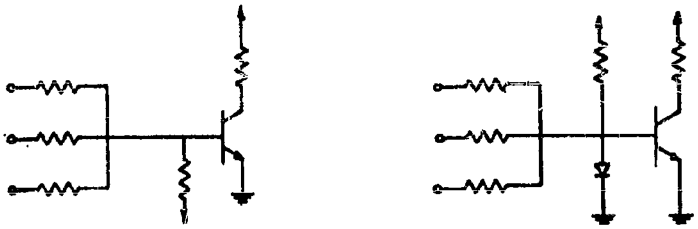
DCTL - NOR

RTL-NOR



DTL-NOR

DTL AND-OR



THRESHOLD RTL

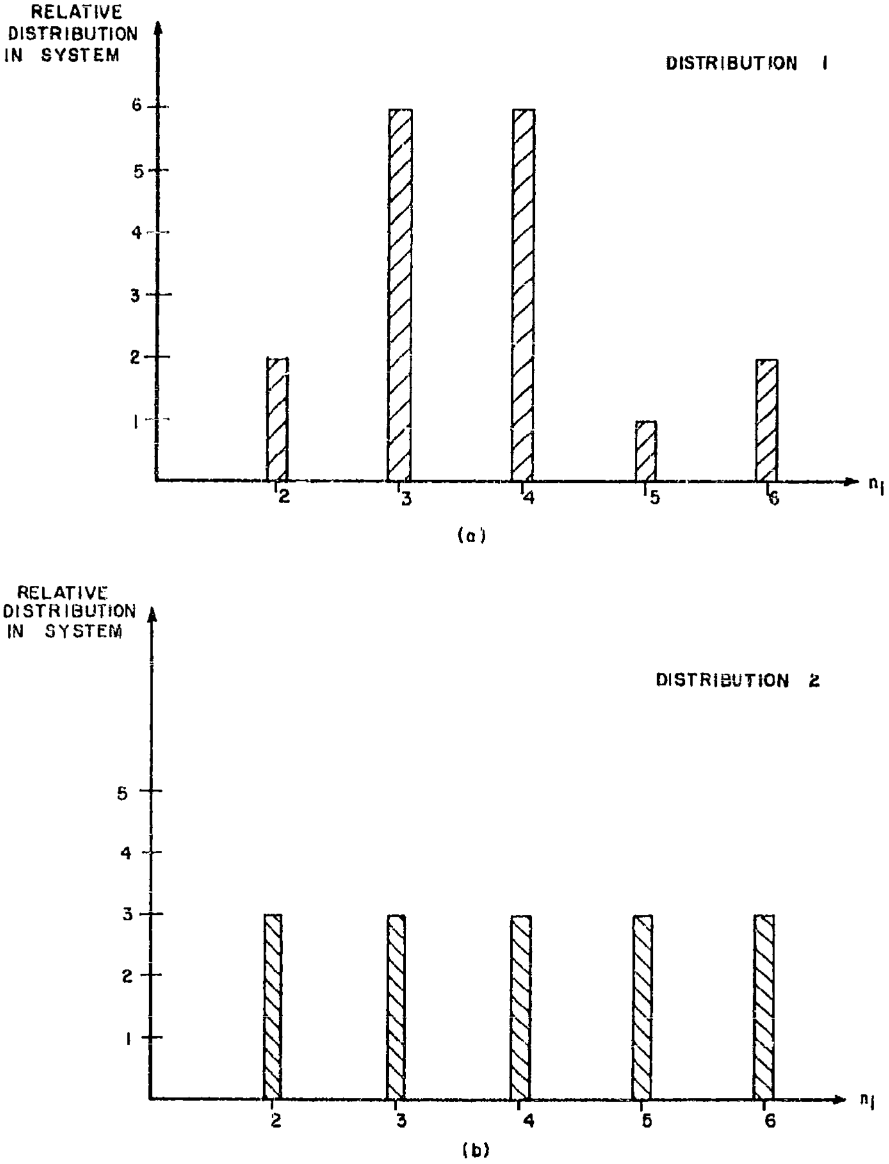
THRESHOLD RTDTL

LOGIC GATES
FIGURE 4

passive elements will be more stable or reliable than the active elements. From this point of view, many of the additional components used in DTL may no longer be required and hence circuit designers may decide to standardize on DCTL configurations. Under the assumptions, this would be a valid choice. On the other hand, a different assessment of microelectronic capability may lead to the choice of a different configuration. Thus, if thin film circuits using discrete active components are considered, reliability of the passive components may prove to be greater than the transistor and thus lead to selection of the DTL configuration. The correct choice can only be determined by comparing various configurations and technologies supplemented by actual system tests over sufficient periods of time to establish reliability criteria with meaningful confidence.

In some cases, it may prove worthwhile to standardize on several configurations. Considering the majority logic function, for example, it would require four resistors and nine transistors to implement the circuit in a DCTL configuration while it would require only five resistors and one transistor if threshold RTL is employed. Considerable tolerance margins can be picked up by the use of a tunnel diode in combination with the transistor in an RTL threshold gate, as illustrated in the bottom of Figure 4. The realization of threshold configurations in semiconductor integrated form may be quite difficult if not impractical with the present state of technology, but ruling out threshold logic can increase system complexity by as much as two to one in certain applications. Thus, is is not inconceivable to assume that standardized circuits may take several forms including semiconductor functional DCTL gates, thin film DTL gates and even conventionally assembled threshold gates. If reliability is to be optimized, there is no reason to believe that such a variety of standard circuits are incompatible with one another.

Once the circuit configuration has been selected, it is necessary to standardize design details such as fan-in, fan-out, power required for stabilization, speed, logic delay, source potentials, etc. The problem is complicated insofar as these parameters are usually not independent. For example, the fan-in number affects speed as well as circuit power dissipation. In order to standardize the circuit design, it is necessary to study system requirements and parameter distribution curves relating to each of the desired circuit properties. To illustrate the point, consider Figure 5a which shows the relative distribution of gates having a fan-in of from two to six for a particular system. The question arises as to how many inputs should be made available in a standardized gate to perform the various logic functions in the



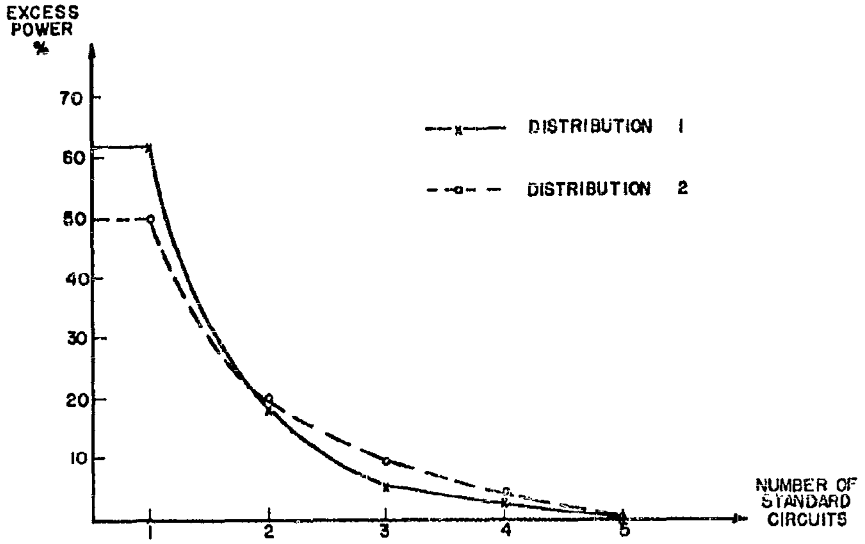
RELATIVE DISTRIBUTION OF CIRCUITS HAVING FAN-IN OF n_i
FIGURE 5

system. Figure 6 illustrates how the system power increases as a function of the number of standard circuits used. For example, if the system is custom designed so that separate gates are made available to handle each of the fan-in requirements, the excess power requirements would be shown as zero in Figure 6 (this assumes that each of the gates is designed optimally for minimum power dissipation). However, if it is desired to use a gate with a fan-in capability of six throughout the system, then the power penalty for standardizing on a single circuit of this type would be 62%, i.e., 62% more power would be required in the system than if the gates had been designed to handle each fan-in requirement with minimum power. However, if two standard circuits are selected, the excess power requirement drops from 62% to 18%, while if three standard circuits are selected, the excess power is further reduced to 5%.

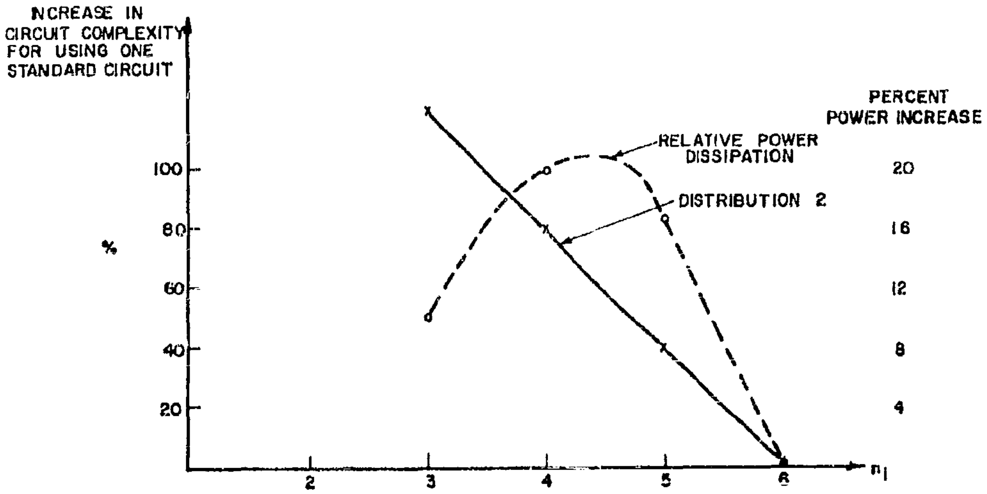
Under certain conditions, it may also be desirable to provide a standard module that does not have the full fan-in capability required by particular circuits in the system but to use tree arrangements in order to handle the increased fan-in requirements. Such measures always lead to an increase in circuit complexity as illustrated in Figure 7. For example, using distribution two illustrated in Figure 5b, if a single circuit with a fan-in capability of six were used throughout the system, no additional circuit complexity would be required although, as indicated above, a considerable increase in power would be necessary. However, if a module with a fan-in capability of four were used throughout the system, the circuit complexity would be increased by 80% under worst case conditions, while using a module of a fan-in capability of three would increase the circuit complexity by as much as 120%. However, it is interesting to note from the power curve of Figure 7 that the system comprised of circuit modules having fan-in's of three would dissipate some 10% less power than the system composed of circuit modules having a fan-in of four. Consequently, many trade-offs have to be made in the standardization process and these trade-offs, in general, will affect both system complexity and system power dissipation. The compromise should be made on the basis of reliability and cost considerations.

4.0 Power Dissipation

Circuit power dissipation is an important factor in reliability considerations because system temperature is directly related to power dissipation and component failure rates are related to both power and temperature. Consequently, it is important to consider how and why power is utilized in electronic circuits. Circuit power dissipation is determined by the amount of



POWER VS. NUMBER OF STANDARD CIRCUITS
FIGURE 6



SYSTEM COMPLEXITY VS. CIRCUIT FAN POWER
FIGURE 7

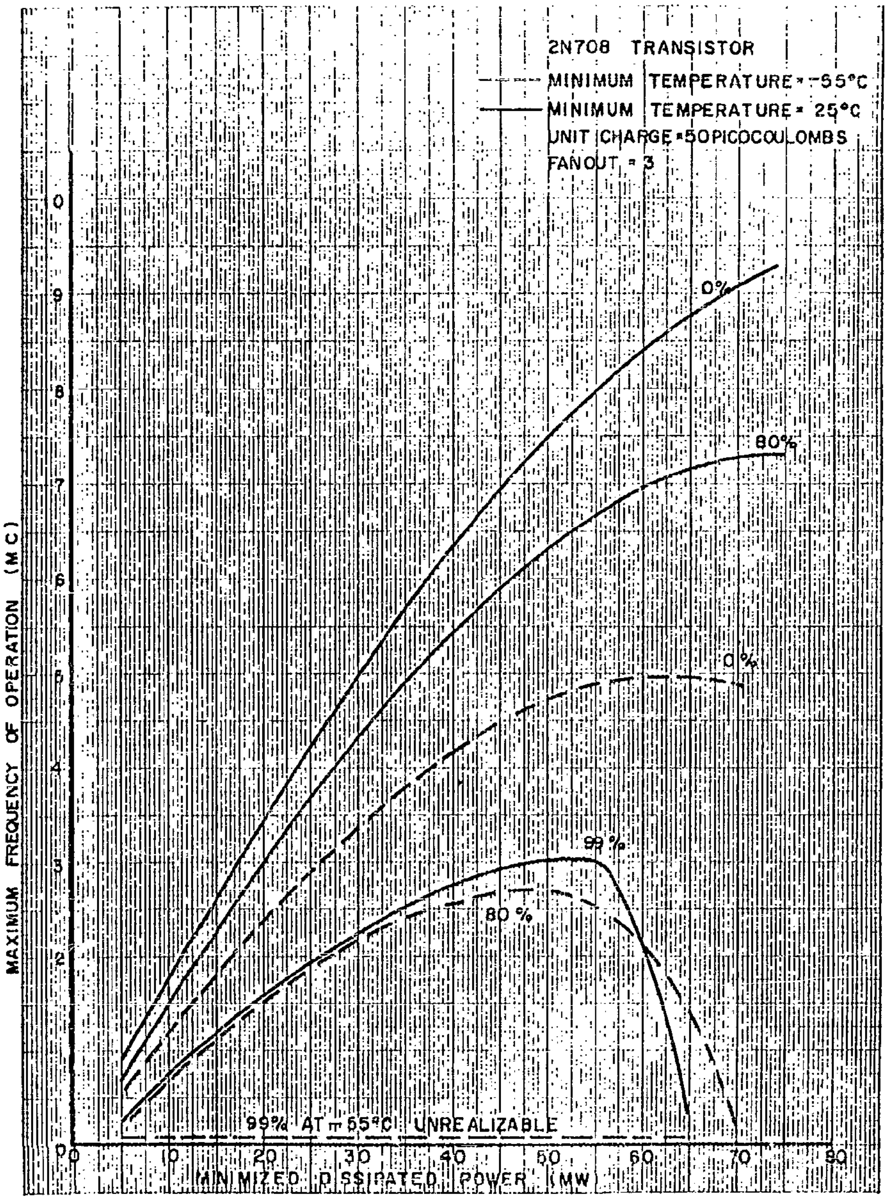
work the circuit must do, which in terms of logic gates implies a power relationship between fan-in, fan-out and speed. However, power is also related to the quality of components used in the circuit.

Figure 8 illustrates curves of power dissipation as a function of circuit operating speed and transistor tolerances for a DCTL gate having a fan-out of three and a unit-load charge requirement of 50 pcmbs. The confidence levels denoted in the curves of Figure 8 relate to the parameter distributions of the particular transistors used in the gate, viz., zero percent implies ideal transistors with no parameter variations (or perfect match) while the curves marked 80% signifies that 80% of the transistors perform properly in the circuit for the particular transistor distribution curves used. It is apparent from Figure 8 that for a wide range of frequency, circuit power dissipation is almost directly proportional to operating speed. In addition, it is seen that as a circuit is designed for greater and greater transistor tolerances at a given speed, the power dissipation increases rapidly. For example, from the curves of Figure 8, if the DCTL circuit is to be operated at temperatures of -55°C at a speed of two megacycles, the power dissipation of the circuit would be approximately 17 milliwatts if all transistor parameter values were exactly on the means of the distributions. However, if the circuit is to be operated without sacrifice of performance and include 80% of the transistors within the parameter distribution curves, the circuit power dissipation would necessarily increase to 27 milliwatts.

Since tolerances play a significant role in determining the power dissipation of a circuit, it is necessary that component tolerances be ascertained with reasonable confidence when microelectronic techniques are used to fabricate circuits. If such information is not available, the circuit designer can only guess at what the proper design should be and in general he will be overly conservative under these circumstances. Over-conservatism in design implies more power dissipation than is necessary. The effect of overdesign on reliability will be considered in the next section.

5.0 Temperature and Reliability

The operating temperature of a circuit depends on its power dissipation, on the thermal conductivity associated with the system configuration and on the ambient temperature. The power dissipation will vary considerably as a function of the temperature range over which the circuit is designed. Since components change in value due to their temperature coefficients, a circuit which is

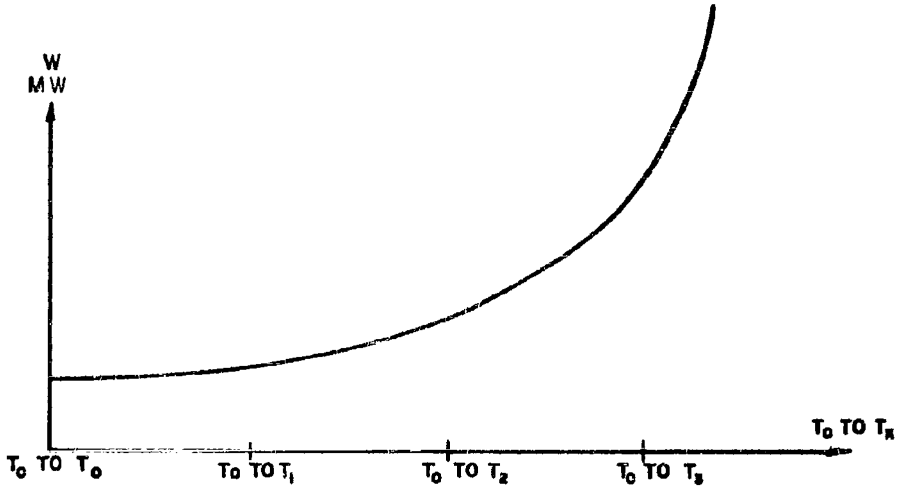


FREQUENCY VS. POWER AT DIFFERENT CONFIDENCE LEVELS
FIGURE 8

expected to work over a wide temperature range must be designed to accommodate the wide spread in component values. (In many circuits, the design can be handled in such a manner that component ratios rather than absolute values of components are significant. However, the ratio principle cannot be applied to active elements such as transistors, or coupling elements such as capacitors, where usually minimum or maximum values are the significant design parameters.) For all classes of circuits, curves showing circuit power dissipation as a function of the temperature range over which the circuit is designed to work may be obtained similar to the one shown in Figure 9. Circuit power dissipation increases as the temperature design range is increased. In practical cases, the power dissipation rises very rapidly at some extreme temperature range; this implies that eventually no amount of additional power can overcome the component degradations and still have the circuit meet performance requirements. It is obviously essential to design circuits well below the range where power requirements rise so drastically.

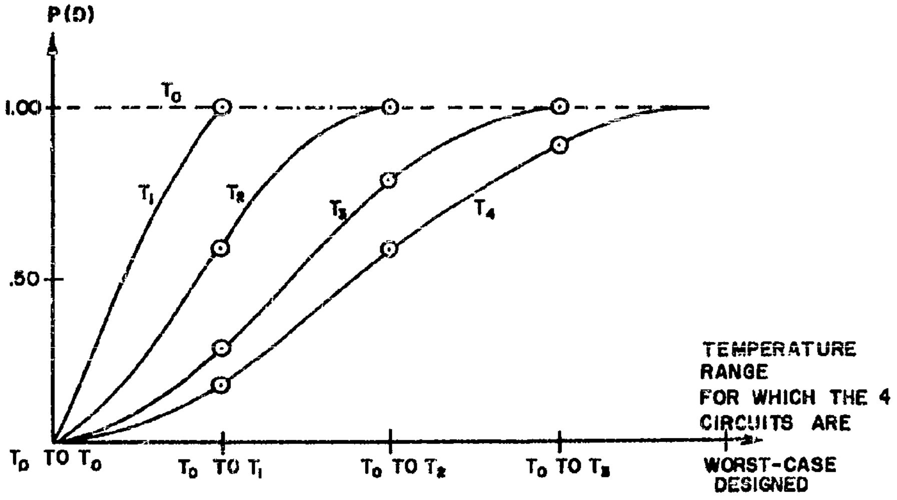
Once a circuit has been designed to meet a set of performance characteristics over a given temperate range, the design can be tested for its probability of successful performance when the operating temperature is different from the design range. With the aid of a computer, the equations of circuit performance may be solved many times by picking component values in accordance with respective component distribution functions relative to the temperature range being considered. This Monte Carlo method of analysis provides results which show the number of times that a circuit does or does not meet its circuit specifications when components are randomly selected in accordance with the distribution functions. A set of curves can then be generated as illustrated in Figure 10. For example, the circuit that was designed to operate over a temperature range of T_o to T_1, assuming rectangular component distributions, would have unity probability of working successfully if the actual operating temperature did not exceed T_1. However, if the operating temperature increases to T_2, due to an increase in ambient temperature or to increased power dissipation, the probability of the circuit successfully meeting its performance specifications drops to 0.6. It should be pointed out that the rectangular distribution is not an unrealistic assumption for fabrication techniques which allow initial selection of individual components. How well the rectangular distributions work for microelectronic fabrication techniques remains to be seen.

The next important step in the reliability analysis is to determine the thermal conduction characteristics of the system in which the circuit is used. Assuming a homogeneous system, the



POWER DISSIPATION W AS A FUNCTION OF "T_0 TO T_X", THE TEMPERATURE RANGE FOR WHICH A CIRCUIT IS WORST-CASE DESIGNED.

FIGURE 9



P(D), THE PROBABILITY THAT A CIRCUIT DOES NOT FAIL DUE TO DRIFT OF COMPONENTS. THE CURVES SHOWN WERE OBTAINED BY ACTUAL COMPUTER SIMULATION OF CIRCUIT FAILURE.

FIGURE 10

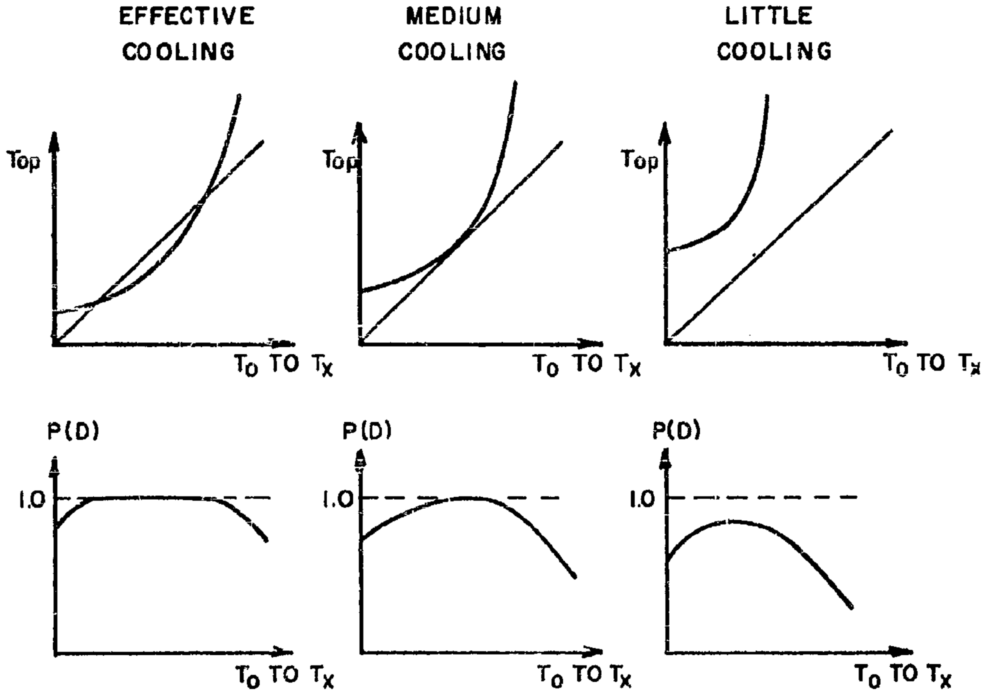
significant equation is

$$T_{OP} = (K)\ (P_{DISS}) + T_A$$

where T_{OP} is the steady-state operational temperature of the circuit, K is the thermal conduction coefficient of the system, P_{DISS} is the steady-state circuit power dissipation and T_A is the ambient temperature. Since circuit power dissipation is a function of the design temperature range, the circuit operating temperature may be related to the circuit design temperature by the equation given above. Curves of operating temperature as a function of design temperature are shown at the top of Figure 11 for different system thermal conduction coefficients. The straight line shown in the curves is the line where operating temperature is just equal to design temperature. It is apparent that a circuit may be designed to operate with 100% probability of success against component variations due to temperature (assuming rectangular density distributions) if and only if the circuit operating temperature is equal to or less than the design temperature. In general, as Figure 11 illustrates, there will be a definite range of design temperatures over which this probability of success can be achieved.

The relationship between operating temperature and design temperature may be used in conjunction with the circuit probability curves of Figure 10 to generate the probability curves illustrated at the bottom of Figure 11 relative to different system thermal conduction parameters. Thus, an optimum range of circuit designs exists wherein the circuit will be able to meet its requirements against component drift due to temperature variations with virtually 100% probability of successful operation. If the circuit is designed for too low an operating temperature, or too high an operating temperature, its probability of successful operation will be less than optimum. It is important to note from Figure 11 that the thermal conduction properties of the system play a critical role in determining how the circuit should be designed.

While the analysis described above has considered explicitly component variations as a function of temperature, initial component manufacturing tolerances can be treated as being equivalent to an increase in operating temperature. This results from the relationship between power dissipation and tolerances. Thus, it is interesting to note that increased component tolerances can be considered equivalent to less effective system cooling. The implication to microelectronics is that packing densities may have to be traded off against component tolerances in order to maintain a given system reliability.



INFLUENCE OF THE COOLING ARRANGEMENTS UPON P(D).

FIGURE 11

Components can change with time as well as with temperature, and as time increases components may fall outside of the well-defined "end-of-life" distributions assigned to them. Such radical drifts in component values are here referred to as "catastrophic" failures. It is well known that catastrophic failures are related to both circuit power levels and operating temperatures. For example, Figure 12 shows a typical set of failure rate curves for resistors as a function of power level and operating temperature. If it is assumed that the probability of successful circuit operation in the face of catastrophic failures follows some form of exponential law such as

$$P(C) = e^{-\lambda t}$$

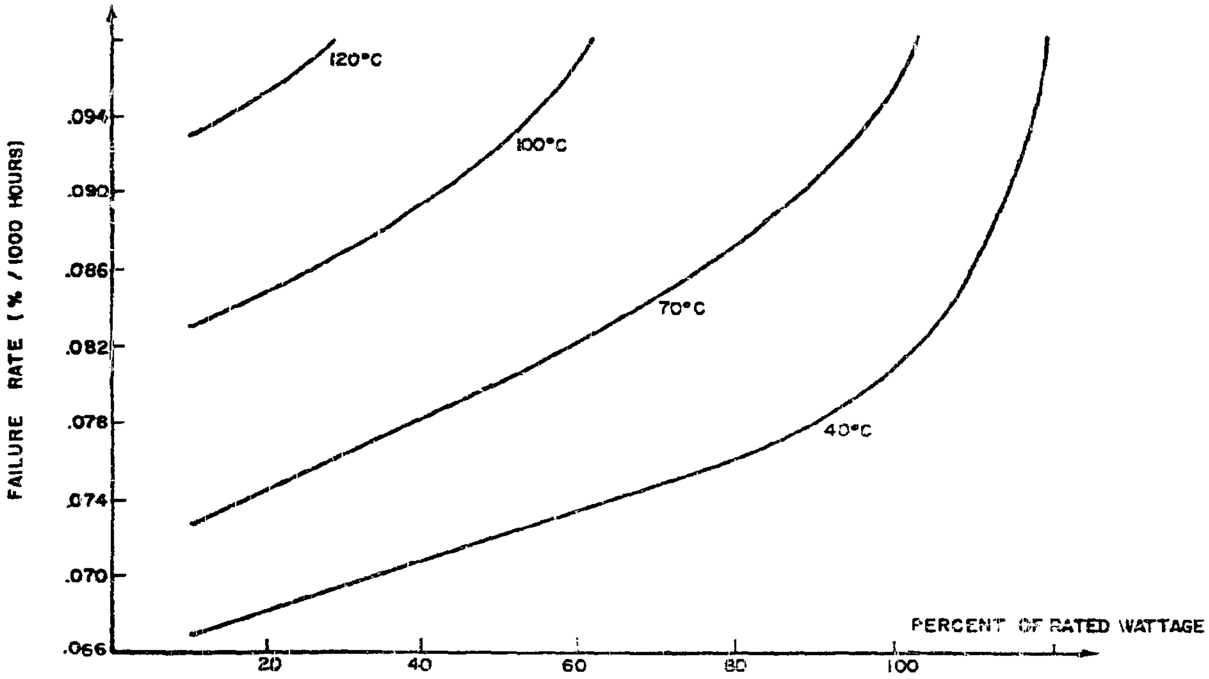
where λ is the catastrophic failure rate of components in the circuit, the over-all probability of circuit success will be given by the joint probability

$$P_S(C) = P(D)e^{-\lambda t}$$

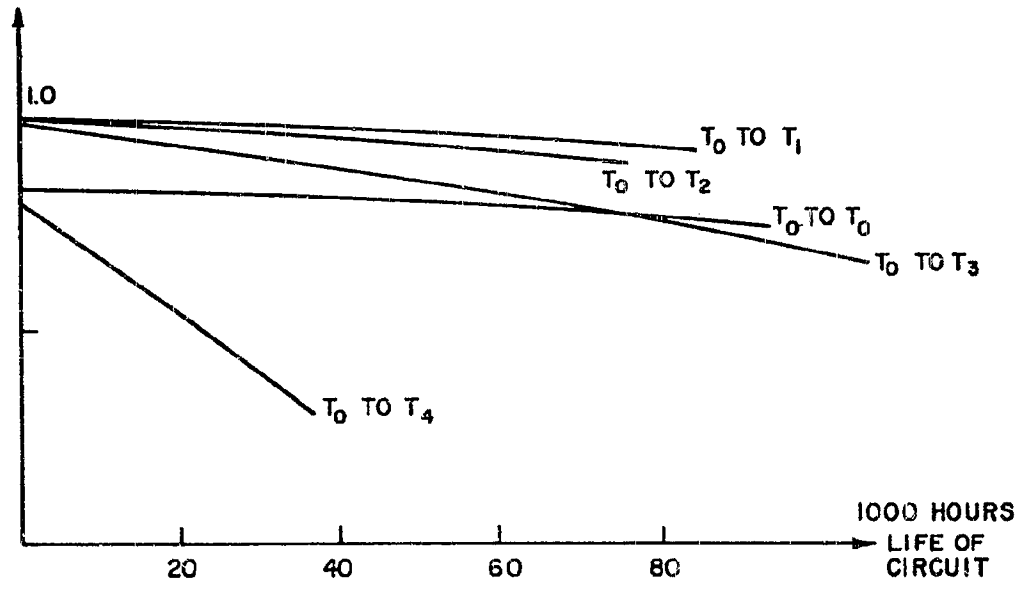
where P(D) has the form illustrated at the bottom of Figure 11. (It is further assumed here that P(D) and P(C) are independent of each other.) Since the catastrophic failure rate increases significantly with increasing temperature, it is apparent that the highest lifetime circuits will be those which can tolerate component parameter variations due to initial tolerances and ambient temperature changes while at the same time operate at the minimum possible temperature levels.

Curves showing the probability of circuit success as a function of time for different design temperatures are illustrated in Figure 13. The circuits which have been designed for temperature ranges from T_0 to T_1, T_0 to T_2 and T_0 to T_3 (where the subscripts 1-3 indicate successively increased design temperatures) start out with a success probability of unity, but the probability of success falls off faster for the circuits which have been designed for the greater temperature ranges. This is due to the increased power dissipation of these circuits and the resultant increase in operating temperature even though the ambient temperature for all the circuits are the same. Circuits designed to operate over the temperature range T_0 to T_4 pay too heavy a penalty in power dissipation even at time zero.

An interesting probability curve is the circuit which was designed to operate at a single low temperature, denoted by the curve T_0 to T_0 in Figure 13. This circuit has been underdesigned



FAILURE RATES FOR VARIABLE COMPOSITION RESISTORS. RESISTANCE VALUES BELOW 50K
FIGURE 12



SUCCESS PROBABILITY OF CIRCUITS DESIGNED FOR DIFFERENT TEMPERATURE RANGES

FIGURE 13

since no provision was made to meet the variation in component values with temperature changes. Consequently, the circuit starts out at time zero with a probability of success less than unity. However, since the circuit was designed for very tight tolerances, it dissipates less power than the wider tolerance circuits and hence runs at a lower operating temperature. This in turn decreases the catastrophic failure rate so that eventually the surviving circuits have an even greater probability of success than those circuits which were "properly" designed initially to take temperature variations into account. The significance of this intersection of probability curves remains to be determined from more quantitative analysis but one may speculate whether it implies that circuits having long-life mission requirements should be deliberately underdesigned, leading to lower initial yield, and then subjected to long burn-in periods before actual use.

6.0 Conclusions

Circuit complexity and operating temperature are critical in determining the reliability of a particular system. In many cases, circuit complexity can be reduced by the use of high speed circuits which may perform many operations serially rather than using slower circuits in parallel. However, high speed circuits require increased power dissipation which, in turn, necessitates a lower packing density in order to maintain reasonable operating temperatures in the system.

Standardization is related to reliability because it influences system complexity and power dissipation. Standardization is necessary for purposes of easier maintenance and lower equipment costs, but should be effected in a manner which does not significantly compromise system reliability. This requires that specification for standard circuits should be as realistic as possible. Overspecification has the same detrimental result to system reliability as overdesign.

The relationship between component properties, circuit power dissipation and system temperature indicates that the use of lower-quality components, viz., components having wider tolerances and greater temperature coefficients, can be considered equivalent to designing a system with poorer heat-transfer characteristics. Thus, it is necessary to know the tolerances of microelectronic components before microelectronic circuit designs can be optimized for system applications. From a reliability point of view, packing densities should not be determined by the size of microelectronic components but rather by the heat-transfer properties of the system.

If tolerances cannot be determined adequately in integrated functional blocks, due to inaccessibility of the fabricated components, it may be desirable to underdesign microelectronic circuits in order to minimize power dissipation and then subject the circuits to long burn-in periods for purposes of eliminating marginal circuits.

A considerable handicap to circuit designers concerned with utilization of microelectronic functional components is the lack of definite knowledge regarding tolerances and failure rates at different temperatures and for assemblies using different fabricating procedures. It would be highly desirable to perform large scale testing of functional assemblies of the semiconductor and thin-film types in order to obtain performance data which circuit designers can use to optimize reliability prior to standardization of the functional block.

7.0 Acknowledgments

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THIN FILM APPROACH TO COMPLEX ELECTRONIC SYSTEMS

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The purpose of this paper is to discuss the status of the thin film microcircuitry art with particular reference to complex electronic systems.

Prior to discussing the state of thin film microcircuitry, the following are presented as examples of what can now be done in this area.

Figure 1 is a single module which may contain 25-30 or more components. The particular module shown has a beryllium oxide top to aid in conducting heat out of the module. Figure 2 is another type of module with a metallic heat shield. There are, of course, many possible configurations of this type but these are typical. There are at this time about sixty different types of modules being fabricated in our facility, and these include digital, analogue, and RF circuitry.

Figure 3 is a ten stage binary counter which has been completed and delivered. This is an example of digital circuitry.

Figure 4 is a three stage 60 mc I. F. amplifier, an example of an R. F. type of circuit.

Figure 5 is a microcircuitized Autopilot Yaw Axis which has been fully qualified and which will be flight tested by the Bureau of Naval Weapons later this year. This is a typical analogue problem.

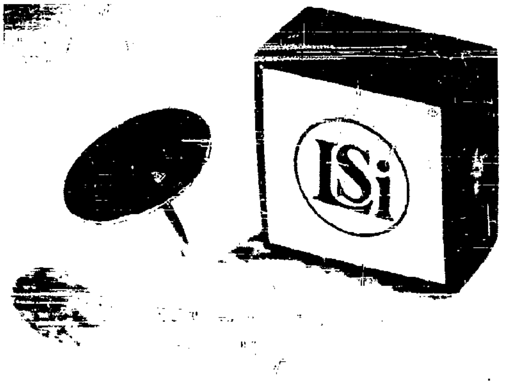

Figure 1

530774-1
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Figure 2

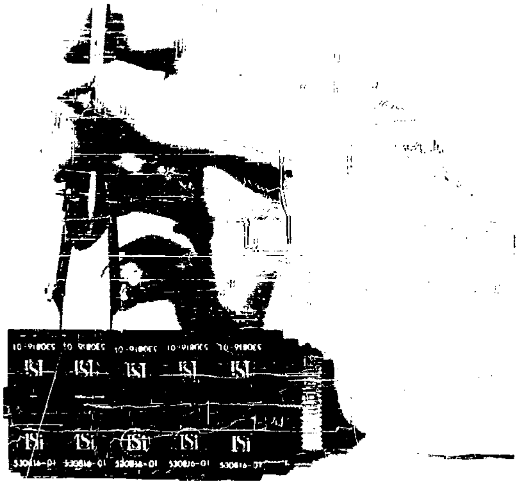
10 PIECES
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Figure 3

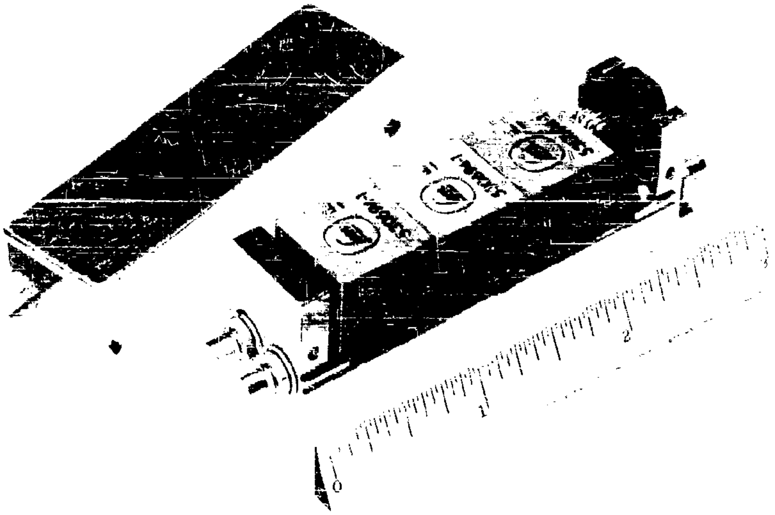


Figure 4

Figure 5

We are just completing a 200 module digital computer for a satellite application, as shown in Figure 6.

These are examples of precision circuitry, fabricated to exacting performance and operational specifications which not only can, but are being made by thin film microcircuitry.

The status of the thin film microcircuitry field could perhaps be typified by the four phase program we currently have underway.

PHASE A (Current)

We are now producing in our laboratory and in our pilot production operation thin film microcircuitry with add-on active elements. We have approximately 50 different types of electronic circuits on test or in fabrication, and are developing a complete thin film system as well as a microcircuitized autopilot. The thin film system is a Digital Data Compiler which contains approximately 200 individual circuits and is, as far as we know, the first system of this type to have been contracted for in this country. The autopilot, the yaw axis of which has been microcircuitized, will be flying later this year in an F8U airplane under Navy sponsorship.

The types of modules with which we are working include digital circuitry, analogue circuitry, and RF circuitry. This to us emphasizes the flexibility of the thin film circuit and the ease with which various types of circuitry can be fabricated to the operational tolerances required by the military. A production machine has been developed and constructed and is in operation, which enables the fabrication of this type of circuitry at a very reasonable cost. This Phase A is our current state of the art phase.

PHASE B

Most of the individual circuits being developed and/or produced under Phase A are deposited onto 1/2" square substrates. Although we have made no effort to standardize substrate size, the circuitry which we have been producing has nearly always required the use of this 1/2" square substrate. Concurrent with our Phase A work we have been improving our masking techniques to the point where we can now work quite easily with 1 mil or less line widths. Our Phase B effort will then include the reducing of the size of the modules we are now fabricating to 1/4" square substrates, still with add-on components. For this reduced area,

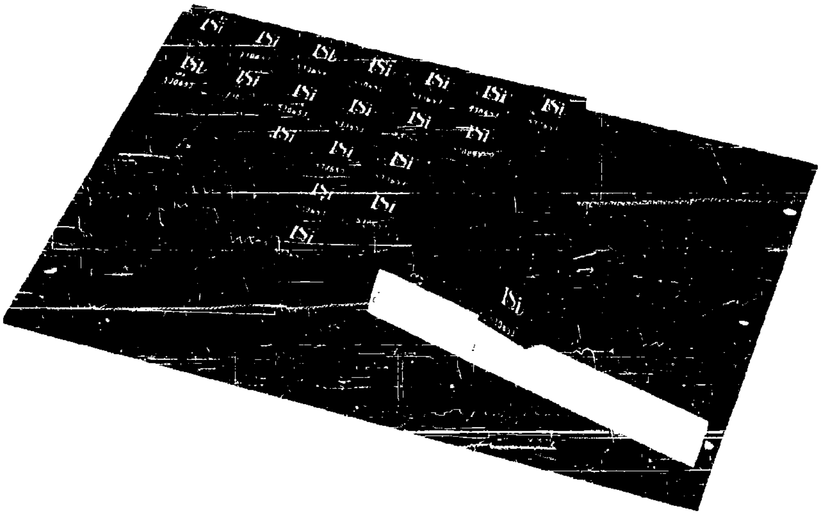


Figure 6(a)

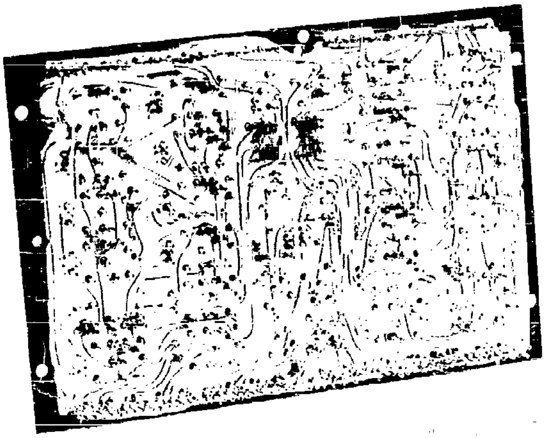


Figure 6(b)

however, we will use chip type transistors and diodes which are now available from a number of transistor manufacturers. These chip elements will be bonded to our microcircuitry by compression bonding techniques. Our production machine, as it is currently operating, will produce 360 microcircuits of the Phase B type in a two hour time cycle.

PHASE C (Hybrid Microcircuitry)

Phase C will include a substantial step forward in thin film microcircuitry, in that the passive components will be deposited onto a semiconductor substrate into which have been diffused the active elements required for the particular circuit being fabricated. This type of microcircuit we have termed the hybrid circuit because it will combine the best features of the so-called molecular circuit, or solid circuit, and of the thin film circuit. The most interesting feature of the molecular circuit is the freedom from having to attach active elements. The passive components of the molecular circuit are quite poor, being unstable and incapable of being diffused to any degree of accuracy. The strong feature of the thin film circuit is the accurate and stable passive components which are absolutely mandatory for high performance military electronics. By depositing the thin film passive components upon a silicon substrate into which active elements have been diffused, the thin film circuit and the molecular circuit have been combined in a manner which should produce a very interesting type of microcircuitry. The active components being diffused into the substrate would, obviously, not have to be attached to this form of circuitry, and leads from the passive to the active components could be evaporated by the techniques we now use to interconnect resistors and condensers.

We are going ahead with the preparation of samples of this type of microcircuitry and should have operating examples in October. We feel it should be possible to slightly reduce the size of this type of microcircuit and estimate that the circuits we are now depositing upon 1/2" square substrates could be deposited on .2" square substrates in the hybrid type of microcircuitry. Our production evaporator would deposit 500 microcircuits of this type within the two hour time cycle.

NOTE: We should emphasize here that it would be highly desirable to interconnect as many of these .2" square microcircuits on one substrate as would be possible and consistent with obtaining reasonable yield values.

PHASE D

Phase D would be what we feel to be the ultimate form of microcircuitry, in which both the active and passive components are deposited by thin film techniques. We currently have Air Force Contract No. AF 33-(657)-7623 calling for the investigation of the properties of single crystal thin film semiconductor material. We are now able to deposit single crystal films of gallium arsenide and germanium and are evaluating this material with respect to depositing active elements. We also have deposited numerous thin film active elements based upon the quantum mechanical tunnelling phenomena which is inherent in extremely thin (50 - 100 A) dielectric films. The Phase D microcircuitry could include active elements of either the quantum mechanical tunnelling type or the semiconductive film type, depending upon the outcome of research efforts with each of these types of films. The passive components would be deposited as they now are of thin films having the characteristics required for the passive components and for the interconnecting wiring. The most important aspect of this type of microcircuitry would be the complete freedom of the choice of materials for the active and passive components. The obvious weakness of the molecular circuit is that all of the components, both active and passive, have to be derivatives of the silicon substrate. This limitation is alleviated to a great degree by the hybrid circuit, and will be completely eliminated by the Phase D or completely deposited microcircuit. This completely deposited microcircuit could be fabricated in its entirety in our production evaporator at a very reasonable cost.

The A Phase of this program is reasonably well in hand, with techniques and processes having been worked out for all steps of microcircuitry fabrication. A production machine has been developed and constructed and is in daily operation in our laboratory. Four additional machines are being fabricated and will be completed by the end of the year. To my knowledge, these are the first such machines to be in operation anywhere.

Following is an outline of our Phase A effort. Lear Siegler, Inc.'s integrated thin film microcircuitry is based upon the end functional requirements of the circuitry in preference to the individual consideration of each component requirement independent of its individual relationship in the overall function of the electronic circuit. This approach revolves around a technique wherein entire circuits are fabricated in a vacuum chamber using the techniques of vacuum deposition of multiplicities of materials on a functionally suitable substrate. The deposition of these materials is carried out in such a manner that complete circuits can be fabricated by the alternate deposition of contact and connective materials, resistive films and dielectric films. We have developed facilities for producing integrated microcircuitry which consists of electrical components deposited by high vacuum evaporation techniques. We currently have in operation a production evaporation system which can be used for quantity requirements.

We are specializing in the type of circuit miniaturization which can be reduced to practice under the current state of the art, and which will enable the present delivery of operable and reliable circuitry. We are delivering today integrated microcircuitry as defined by the Committee on Microcircuitry of the Navy Department. Integrated microcircuitry may be defined as the deposition of miniaturized components by one of several processes, thereby producing electronic circuitry with characteristics which are amenable to calculation, and which can be predicted with a minimum amount of experimental adjustments. We are depositing the passive components of the integrated microcircuit by high vacuum evaporation. We are embedding, or otherwise attaching, the active elements. Looking into the future, we have a current development program in which we are evaporating single crystal film material. We are expecting support for this effort, and within one or two years we should be able to deposit the active components as well as the passive components. While we realize this development has no effect on current programs, it should be nevertheless of interest for future circuit consideration.

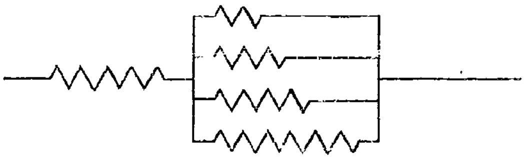
We are depositing nickel-chromium resistive material. Our staff personnel have had many years of experience in the deposition of various types of resistive materials, and there is absolutely no question that the nickel-chromium film materials are superior to any others when stable and predictable resistance elements are to be produced. Such materials as tin oxide, chromium, chromium-titanium oxide, etc., do not compare with properly deposited nichrome. We deposit nichrome onto a hot, soft, glass substrate. The temperature of the substrate is adjusted to a value which insures complete film crystallization during the evaporation process. If this precaution is not taken, an amorphous or partially crystalline nichrome film will result, and the resistors thus prepared will not be stable. Our personnel have deposited tens of thousands of nichrome resistors, and we are able to accurately predict total resistance, thereby eliminating post evaporation tailoring to bring the circuits into specification.

In order to properly contour the resistance elements, we evaporate through very accurately prepared metal masks. We have, on our staff, a scientist who has spent more than twelve years in this field, and who is one of the leading designers of evaporation masks for depositing circuitry. The accuracy of the mask obviously determines the accuracy of the various resistors in a given microcircuit when precautions are taken to minimize the non-uniformity of the evaporation field. Here again, the experience of our personnel is directly applicable to this problem, and by measuring one resistance in a microcircuit, it is possible to very closely deposit the remaining resistances to a reasonable tolerance at the same time. By "reasonable tolerance" is meant a value of two to five percent.

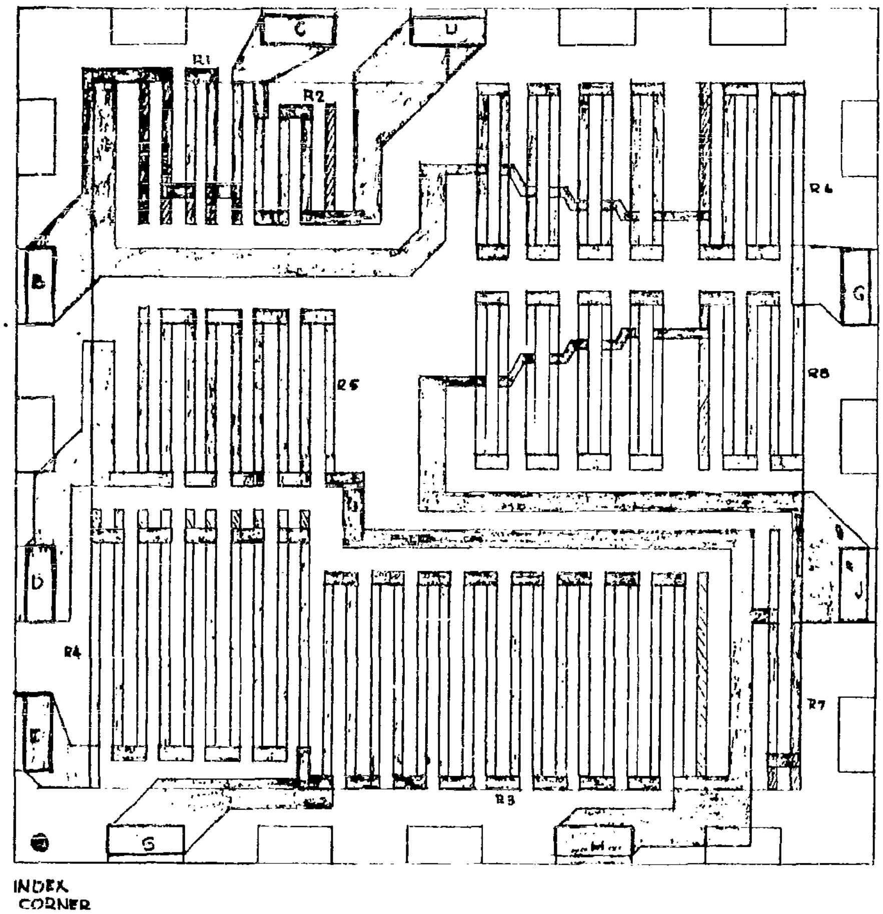
The design of vacuum deposited resistors is of substantial importance to the fabrication of useful microcircuitry. An inadequate understanding of design considerations can produce problems in mask fabrication, problems in the vacuum deposition and, finally, poor electrical characteristics in the resistors, once the circuit has been deposited. One serious problem arising from poor resistor design is the unreasonable wide range of resistive value deviations, once the deposition of the resistor on any one substrate has been completed. However, the design considerations can be included in the layout of a resistor pattern and these will minimize the problem areas to a point where very dependable resistor plates can be obtained. Using the design considerations which have been perfected here at Lear Siegler, Inc., Solid State Physics, resistor patterns are being produced with over 25 stable resistors all with tolerance ranges of 2% to 5%, and these resistor patterns can be obtained directly from our Multiple Vacuum Coater as well. Resistor values from 15 ohms to 150,000 to 200,000 ohms are being made as a matter of practice. At least in a few cases resistors have been fabricated that have operated satisfactorily for reasonable periods of time with 4 watt power dissipation.

Figure 7 shows the resistor side layout of a typical microcircuit substrate. This layout includes 8 resistors ranging from 2,800 ohms to 33,000 ohms. It should be noted that all resistor bars are of the same width. The variation in resistor value being obtained by varying the length. It should also be noted that all resistor bars are not parallel and where possible resistor patterns are adjacent to each other allowing the parallel bar pattern of 1 resistor to continue on from the parallel bar pattern of another with the same spacing, these design details permit greater accuracy in the fabrication of stainless steel masks and also provide a much simpler piece of artwork to be made on the drawing board. Resistors of 5% tolerance can be evaporated to value. Resistors of 1% must be evaporated slightly low and tailored upward to the desired value after the deposition. This tailoring is performed by cutting one of a pair of parallel resistor paths. Resistors R-6 and R-8 in Figure 7 show such parallel resistor paths for tailoring purposes. The four pairs of tailoring loops on each of these two resistors provide tailoring capacity up to 15% in one 1% increment. Cutting one of the parallel paths in the first set increases the total resistance of R-6, for example, 1%. Cutting one loop in the second set would increase the total resistance 2%. Cutting the third set would increase it 4%, and the last set provides an increase of 8%. Therefore, with combinations of these values any % increase from 1% to 15% in 1% increments can be obtained.

Other means of providing tailoring patterns for 1% resistors which have an advantage in size and some resistors where there is low wattage dissipation is indicated below:



A group of 4 or 5 resistors of specific values are placed in parallel. This group in series with a larger value resistor pattern can be utilized by cutting various combinations of these parallel resistors, resistance increases in 1% increments can thus be obtained. This method of cutting out specific resistors thereby changing the total of the remaining parallel path is used because generally it is not practical to attempt to adjust resistance value by cutting away portions of a specific resistor. Partial trimming on a specific resistor mechanically usually causes hot spots in the film or instability of resistance values. Resistors to a closer tolerance may have to be adjusted after evaporation. This adjustment


C
D
R1
R2
R6
B
G
R5
R8
D
J
R4
R7
E
R3
S
H
INDEX
CORNER

Typical Layout of Resistor Side of Microcircuit Substrate

Figure 7

procedure is straightforward. After evaporation, our resistance elements are coated with a layer of silicon monoxide to minimize surface oxidation and contamination.

Capacitors are also evaporated and can be made with a capacity per layer of as high as 2,000 micro microfarads per square centimeter. The dielectric we employ is silicon monoxide or other suitable material. The dielectric evaporation process has been well perfected, and a yield of substantially 100% can be predicted for capacitors having a "Q" of 100. Electrodes for these capacitors are gold, and are evaporated as are the connections between the resistors and capacitors. Terminal connections are also evaporated of gold, thereby forming a microcircuit on the soft glass substrate which is essentially one integral piece.

Interconnections are always a problem with a microcircuit, particularly since they must usually be used in conjunction with non-microcircuitized elements. For this reason, each microcircuit application must be considered individually.

In practically all cases, volume reduction of from 5 - 10 times can be realized through the use of Lear Siegler, Inc. integrated microcircuitry.

Current techniques are adequate for evaporating, or otherwise depositing, the passive electronic components required for an integrated microcircuit. An evaporated nichrome film, for example, produces an excellent resistance element when it is deposited upon a suitably prepared hot substrate. Dielectrics composed of films of metallic and non-metallic materials are suitable for deposited capacitors. Interconnecting wiring can be evaporated gold-nichrome combinations or aluminum. Memory and logic elements for digital computation requirements can be fabricated from laminates of nickel-iron magnetic films and thin film conducting elements as may be required. However, when a transistor is required in a microcircuit, the current practice is to use some form of uncased standard element and to embed, or otherwise attach, this uncased element to the microcircuit substrate. A properly prepared uncased transistor is not an inexpensive component to start with, and the handling costs of inserting it into a microcircuit make it a very expensive portion of the assembly. The question of reliability must also be taken into consideration, particularly since one of the prime objects of the integrated microcircuit is a substantial increase in circuit reliability. This increase in reliability is a possibility because the evaporated components in a microcircuit form a molecular bond with the substrate and, in effect, form a circuit which is actually one integral piece which cannot be separated by exposure to vibration or other extreme environmental conditions. However, when a transistor or diode is inserted into a microcircuit, it is a separate part which must be fastened to the substrate, and it has leads which must be connected to the remainder of the microcircuit by pressure bonding, or by some other fastening technique. While it is possible to handle this active element insertion in a reasonably satisfactory manner, it is not possible to prevent it from being the most vulnerable portion of the microcircuit from the standpoint of reliability.

What is required is some method by which transistors and diodes can be deposited directly onto a microcircuit substrate in a manner similar to that now used for resistors and capacitors. If this could be done, a completely integrated microcircuit could be deposited, representing a very substantial step forward in circuit miniaturization and reliability.

Realizing this requirement, Lear Siegler, Inc. started a program some two years ago to develop means for depositing single crystal semiconductor film materials. This program has met with some measure of success, and numerous samples of single crystal film materials have been prepared. The ability to deposit single crystal semiconductor film material is the first step toward the development of transistors and diodes which can be evaporated into an integrated microcircuit.

We are of the sincere opinion that a solution must be found which will eliminate the necessity for inserting uncased transistors and diodes into integrated microcircuits. Not only are these uncased active elements quite expensive, especially when all handling costs are taken into account, but the need for using them prevents the obtaining of maximum reliability or size reduction from this form of microcircuitry. Conversely, the availability of techniques for depositing film type active elements would make the integrated microcircuit a highly reliable and attractive solution to microcircuitry requirements for current electronic equipment to meet the most stringent operating specifications.

PROTECTIVE ENCAPSULATION STUDIES

The question of environmental protection of our thin film circuitry has received a considerable amount of attention in our laboratories. We have at our disposal a rather well equipped organic laboratory specializing in the formulation of particular types of temperature resistant protective coatings and high polymeric casting resins of one kind or another. We have developed a series of casting resins to be used in conjunction with our thin film circuitry.

The casting resins which we are working with encompass the general chemical families of epoxies, polyurethanes, polyesters and sulfide modified epoxy compositions. We have also worked with a number of internally plasticized compositions which are based upon the co-polymerization of long chained organic acid anhydrides with epoxies which result in polymeric compositions which range in hardness from the very soft down in the 20 to 25 shore durometer to hard materials in the 100 to 110 shore durometer category. These compositions have the advantage of being both flexible and heat resistant so that one is able to employ them in high temperature environments with little difficulty from a depolymerization or weight loss effect. In addition to these resin formulations we have also done considerable work in the area of room polymerizable silicone rubber compositions. These silicone rubber compositions are usable over a temperature range of -70° C to +175° to 185° C. These silicone polymers are capable of being used either as casting resin per se, or to provide a flexible foundation by applying them over the outside contours of a circuit followed by encapsulation with one of the above mentioned polymer compositions. Such a system has proved very beneficial when we have been faced with the problem of encapsulating components which are quite pressure sensitive and respond adversely to the pressure exerted by polymer systems having as little as 2 to 4% volumetric shrinkage upon curing.

Extensive work has been done on filled polymer systems utilizing such film materials as Stupilith, aluminum oxide, silica and beryllium oxide. These filler materials are used to modify such properties as volumetric shrinkage, hardness and thermal conductivity. The effect of these fillers on the viscosity of the monomer solutions, the physical properties of the cured polymer and the effects on the physical properties of the cured polymers have been carefully studied.

Within our series of experimental polymer materials are several foam plastic formulations encompassing both foamed epoxy resins, foamed polyurethanes and foamed polyester materials. These foams are used when weight saving is of paramount importance. However, a judicious choice, many times, must be made since foam materials are very poor heat dissipation polymers. We are, however, working with formulations which suspend microscopic particles of beryllium oxide in the foam which tends to increase its thermoconductivity without substantially increasing its weight. We are also studying formulations where micro-balloons of polymeric alpha-methyl-polystyrene are suspended in epoxy formulations with a subsequent decrease in density of the material without substantial decrease in thermal conductivity. The question of polymer weight loss at 100°C to 125°C in a vacuum of 10^{-6} millimeters has been pursued in the organic laboratory quite thoroughly and at the moment individual formulations in the series discussed above indicate that weight loss under these conditions varies from .75% for several of the individual formulations to as high as 9% for some of the other individual polymers. Thus, we find ourselves in the position of being able to package our thin film circuitry in environmentally resistant polymeric materials which are suitable for space environments and practically all types of environmental conditions which are required by various Government Agencies. We first coat our completed circuit with silicon monoxide to provide as good a protective coating as possible with this technique, followed by encapsulation in one of the polymeric materials mentioned above. Thus, on the samples which we have put through all the environmental conditions called out in MIL E-5400, we have not, as yet, had one single failure due to the effect of any environmental change. We have also carried on considerable work in the plating and evaporation of various shielding formulations to our high polymer plastic materials, with the result that we find ourselves in the position of being able to provide an adequate shielding film which adheres to the plastic surface with great tenacity with little difficulty. Our organic laboratory is in a position to evaluate the development of protective and encapsulant compositions in fields of silicones, epoxies, polyesters, polyurethanes or the vinyls, and these would all include foamed and special conductivity compositions.

The Electronic Systems Problem

The problem in fabricating a microcircuitized system is one of being able to precisely duplicate existing or new electronic circuit designs. Here, the thin film approach offers complete flexibility in the fabrication of specific circuit designs. Whereas design compromises may be made which will enable a more compact microcircuitized system, such design compromise is not mandatory.

Particularly at this stage in the microcircuitry art, it is often desirable to microcircuitize existing systems without having to expend the time or money required for a complete circuit redesign. The systems shown in Figure 5 and in Figure 6 were handled in this manner. The available circuits were miniaturized, by the processes described in this paper, on a component by component basis.

In one sense, the problem of system microcircuitizing is always one of being able to exactly duplicate the circuit designs involved with the required accuracy and stability. When this can be done, the system engineer has the freedom he requires to produce an advanced system sufficiently compatible with, or in advance of, the current state of the art to enable his fulfilling his design objectives. The problem of active elements is a critical one at this stage of the development of microcircuitry and it has been our experience that the people who want a system for a "real" application will want to specify a definite make and type of transistor or diode concerning which they have some prior reliability history. With the thin film microcircuit any type of active element can be supplied from the bare chips to fully canned components.

The interconnect problem is still one which must be solved for each system design. Figures 8, 9, 10 and 11 show the method used in the digital computer shown in Figure 6. Here specially designed and fabricated multiple layer interconnect boards were used. These boards are integrally welded, and the modules are welded into the boards to produce an all welded system. Smaller assemblies, such as shown in Figure 3, may also be used when the system complexity is not too great. The main point to watch is that electrical connections are not multiplied too much to obtain the desired serviceability. For example, in the assembly shown in Figure 9, each module may be replaced at least six times.

Substrate size is another important system consideration and this is purely a matter of yield. This is a matter for each supplier to work out for himself, after he has produced his type of microcircuitry in reasonable quantities. It would be better to produce relatively small substrates with a high yield, than a larger substrate with very low yield. It would not be wise to use large substrates to achieve a less complex interconnect board at the expense of an abnormally low fabrication yield. There is a balance between yield and interconnection complexity which must be satisfactorily worked out. Lear Siegler, Inc., at this writing, does not plan to use substrates larger than one inch square. On a substrate of this size we would deposit over 100 components.

The producing of system circuit modules for a reasonable cost is another "must" for system microcircuitry. For this purpose Lear Siegler, Inc. has developed the semi-automatic evaporator shown in Fig. 12.

This machine can produce thin film circuitry in substantial quantities for a reasonable cost.

In summary, the thin film approach to microcircuitry for advanced systems offers the following:

a. Complete latitude in circuit design.

b. The deposition of accurate and stable components.

c. The selection of any desired active elements, encapsulated or unencapsulated.

d. Complete freedom in choice of substrate size and of interconnection methods.

e. Economy and simplicity of tooling.

f. Economy and ease of fabrication with relatively simple production equipment.

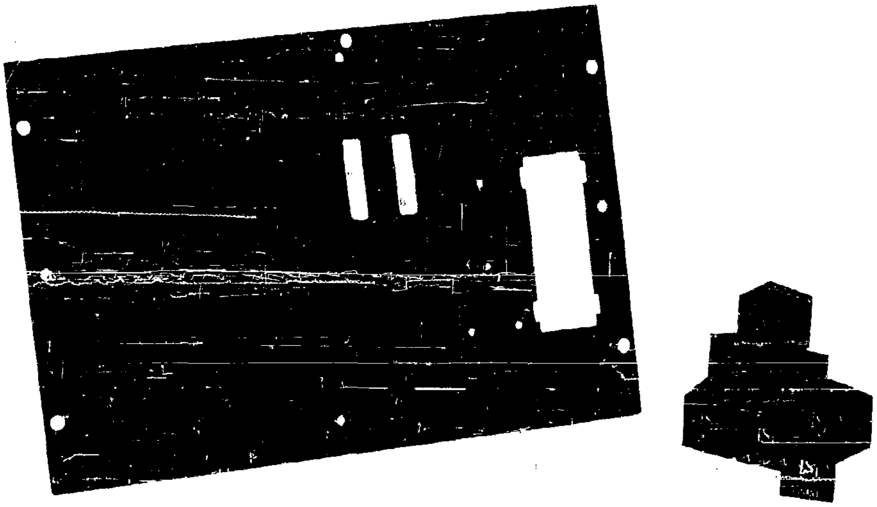


Figure 8

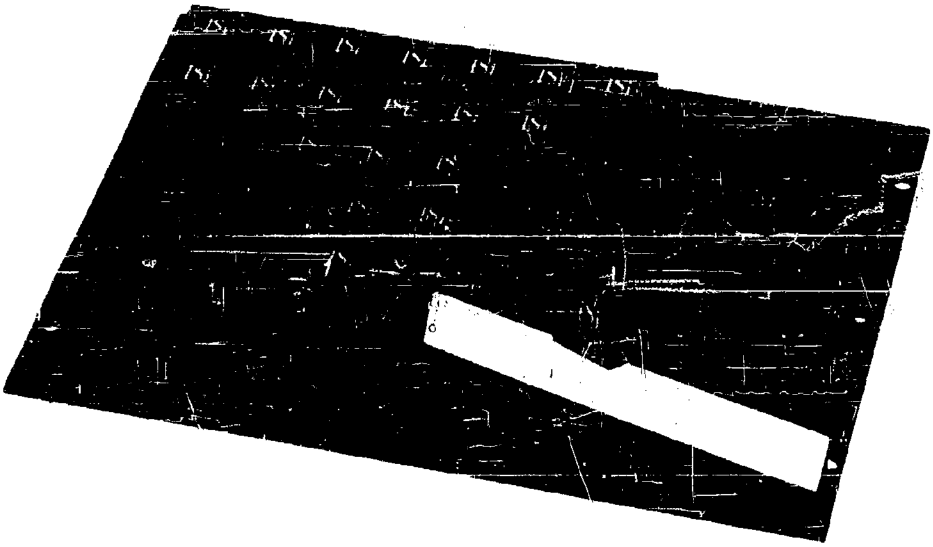


Figure 9

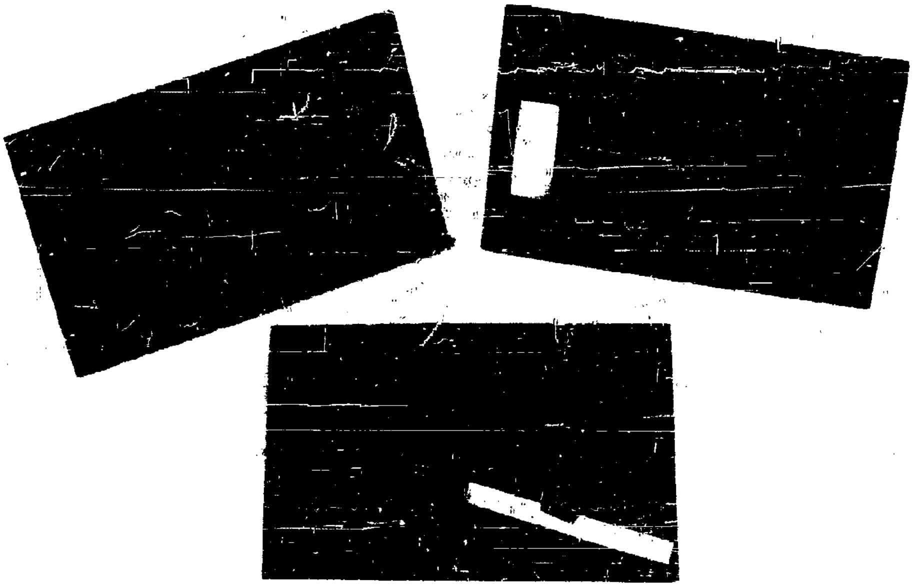


Figure 10

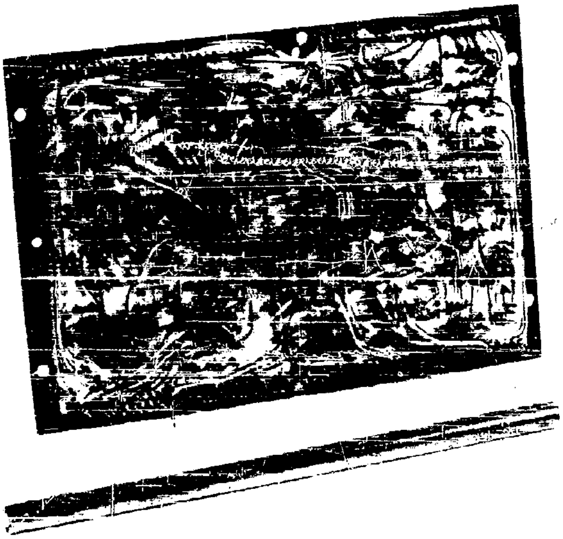


Figure 11

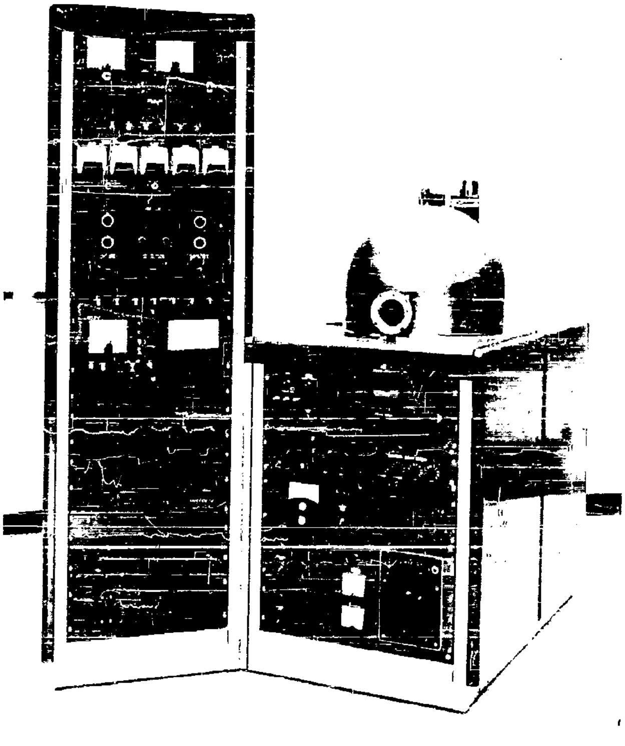


Figure 12

A 1.5 WATT MOLECULAR SERVO AMPLIFIER

M. W. Aarons
Norden Division of United Aircraft Corporation
Norwalk, Conn

Circuit Theory

The circuit to be described was developed with symmetry of element utilization in mind, in order to minimize morphologic problems associated with semiconductor fabrication. It is a differential class A power amplifier.

With reference to the circuit diagram (Figure 1), transistors Q_1 through Q_4 form a differential high impedance voltage preamplifier. Transistors Q_5 and Q_6 are emitter follower driver stages, which are zener diode coupled to the push-pull power output stages (Q_7 and Q8). Resistors R_{11} and R_{12} provide thermal stabilization for the power stage and guarantee that the zeners are broken down.

The open loop gain of the differential forward amplifier (Q1 through Q8) is greater than 2,000. The closed loop-gain, however, is determined by resistor ratios in the differential feedback network: R_1 through R_4 and R_{13} through R_{20}. The over-all gain is precisely specified to be 200 by means of this technique.

D.C. operation points are stabilized by the common mode feedback amplifier consisting of Q_9 and Q_{10} with resistors R21 through R_{26}. The signal across the output is differentially summed by R21 and R22 cancel-

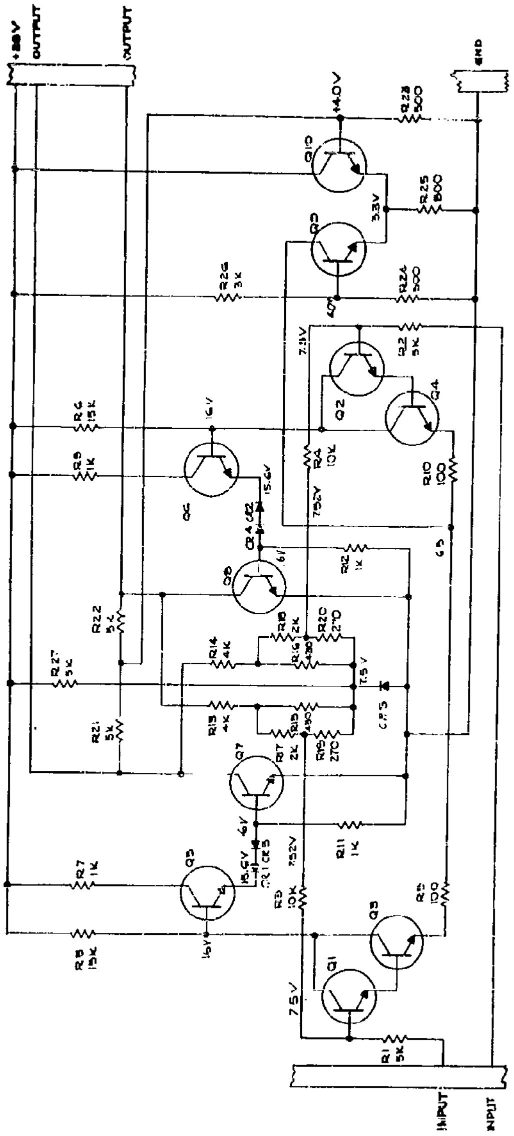

+28V
OUTPUT
OUTPUT
GND
INPUT
INPUT
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
R1 5K
R4 10K
R10 100
R11 1K
R12 1K
R22 5K
R23 500
R25 800
R26 3K
R27 5K
R21 5K
R13 4K
R14 4K
7.5V
14.0V
3.3V
15.6V
16V

Figure 1

COMPONENT CIRCUIT DIAGRAM OF MOLECULAR SERVO AMPLIFIER ling the AC components. The D.C. component is then amplified and applied to the emitters of the differential input Darlington pair.

The method of isolation which consists of back-to-back junction surfaces alters the actual circuit operation by inserting distributed diodes in a complicated manner within the circuit; such that a more exact circuit configuration is shown in Figure 2.

Topology

Since our circuit must deliver sizeable amounts of power, the output stage received a great deal of attention. In conventional power transistors the bulk of the collector body is of very low resistivity. Modern N on N^+ epitaxial planar diffused devices are good examples of this geometry. In crystal circuits it is difficult to achieve this result and maintain a collector breakdown of 120 volts. The motor our circuit drives requires 94 volts peak-to-peak and 120 milliamperes peak current.

An analog device for designing crystal circuit components was developed to solve this problem. Graphs were plotted from data obtained from 200:1 scale models of planar power transistors. Emitters and collectors were constructed of aluminum foil using tape to mask surfaces between collector pads. Solutions of NaOH were mixed in different concentrations to simulate substrate material of 1, 2, 3, and 4 ohm-cm bulk resistivity. The depth of the solution was varied in 0.1 inch increments, simulating 0.5 mil variations in the depth of the collector region. The models were also modified to vary the length of emitter and collector junctions, and the separation of these junctions. Figure 3 is a typical plot of the data, while figure 4 shows the actual structure in a crystal whose edge has been beveled and stained to reveal the internal junction contours. The successful topological inversion of the power transistor structure is unquestionably one of the most important achievements of this program.

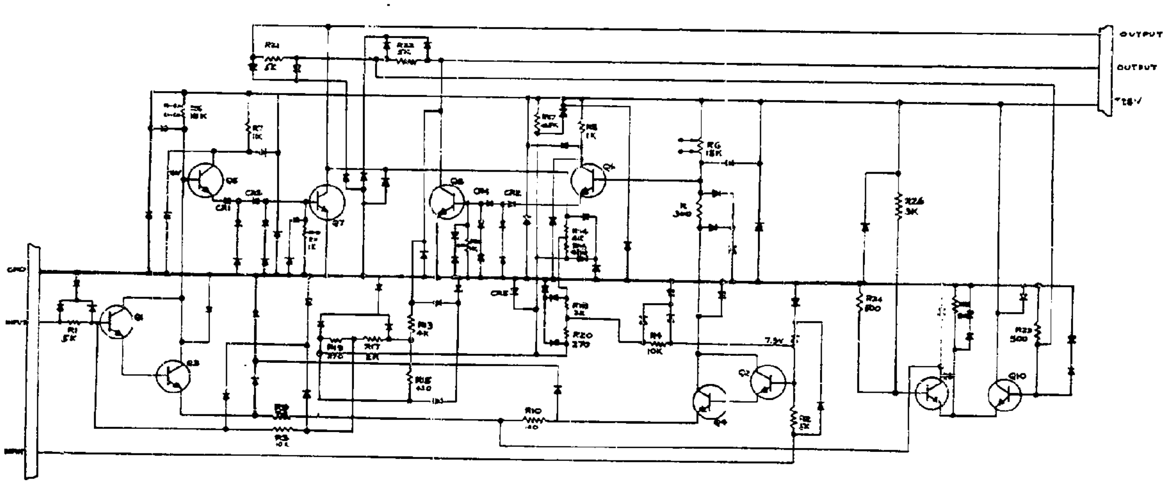

OUTPUT
OUTPUT
+28V
GND
INPUT
R1
5K
Q1
Q3
Q5
Q7
Q8
Q4
Q2
Q10
CR1
CR4
R7
1K
R21
5K
R22
5K
R17
2K
R19
270
R13
4K
R15
430
R10
40
R5
R18
3K
R20
270
R14
4K
R4
10K
R17
68K
R8
1K
RG
15K
R
340
R26
3K
R24
800
R23
500
7.5V

Figure 2

MORE EXACT CIRCUIT CONFIGURATION AS A RESULT OF THE DISTRIBUTED DIODE PLANES INTRODUCED IN SEMICONDUCTOR FABRICATION

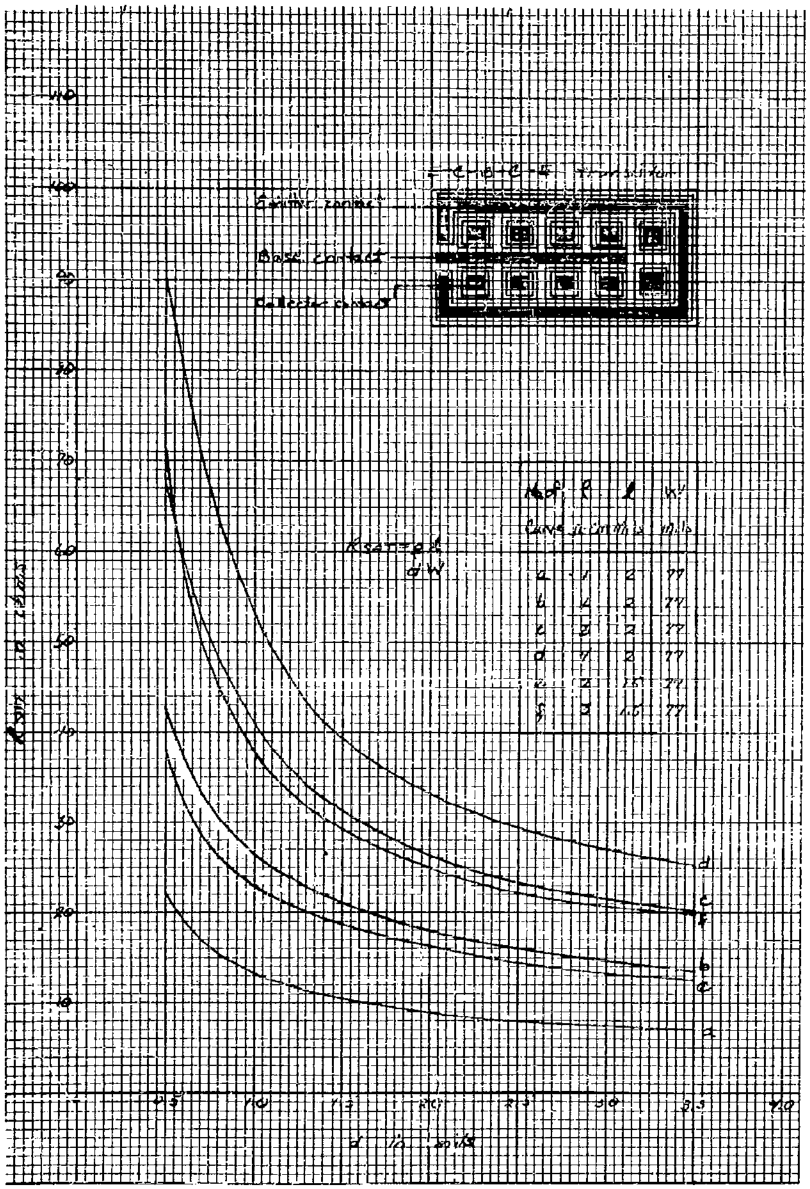


Figure 3

FIELD PLOTS OF POWER TRANSISTOR CHARACTERISTICS
AS OBTAINED FROM ANALOG STUDIES

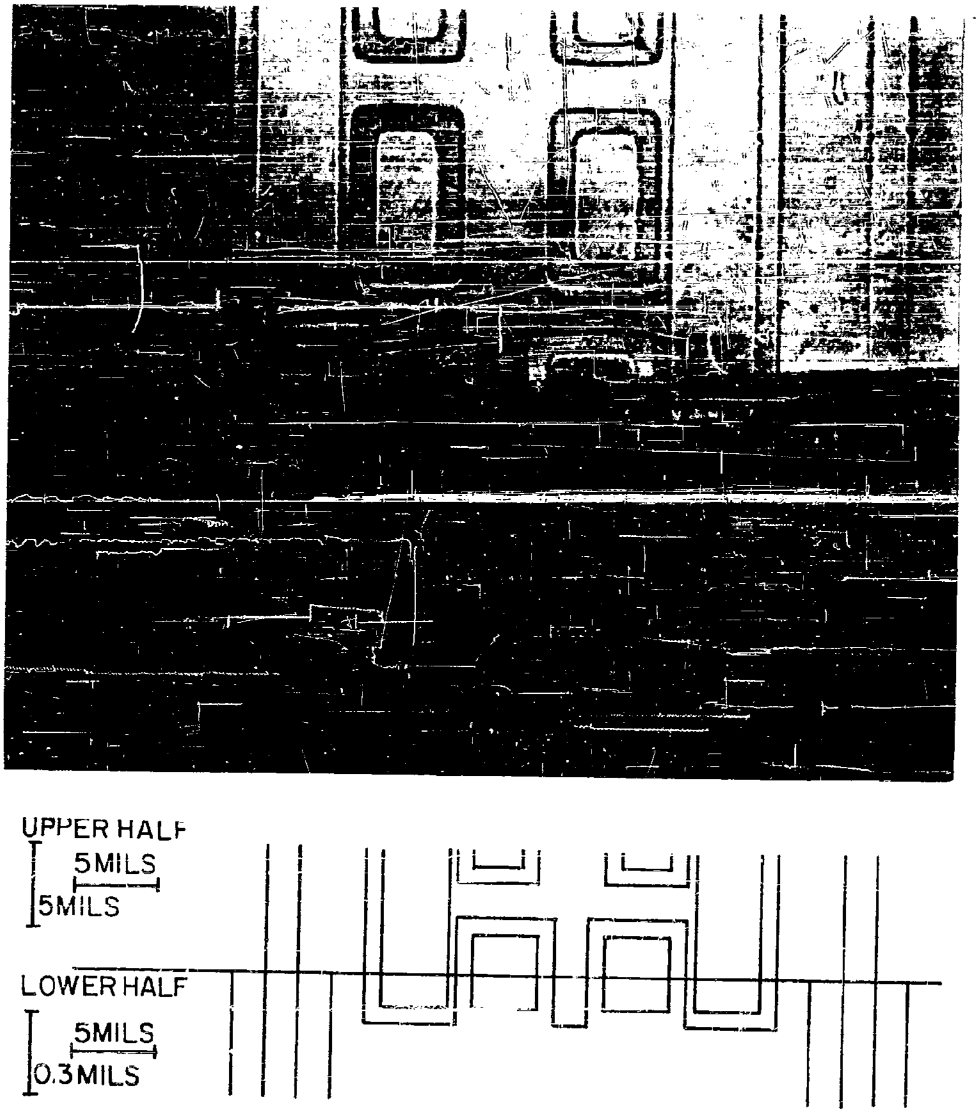

UPPER HALF
5MILS
5MILS
LOWER HALF
5MILS
0.3MILS

Figure 4

MICROPHOTOGRAPH OF POWER TRANSISTOR JUNCTION CONTOURS AS VIEWED ON A BEVELLED AND STAINED EDGE OF THE CRYSTAL

A morphologic algorithm was developed so that complex electrical circuit designs could be translated into topological arrangement of the elements within a crystal by means of simple sets of rules. These rules eliminate interconnection cross-overs and restrict elements with critical interconnection lengths to be close together on the block. As a consequence we can produce radically different crystal geometries for a given circuit in a minimum time. Figure 5 is one example of the many topological solutions applicable to the servo amplifier circuit of Figure 1.

Due to the ambitious nature of our program (an entire electronic system in one crystal of silicon) we were not certain whether process technology was sufficiently advanced to enable initial good yields. We therefore chose a morphologic design which dissected the amplifier (by symmetry) into 4 distinct circuits (see Figure 6). An interconnection scheme was developed which allowed us the following choices. The first choice was interconnecting within each independent circuit then dicing the wafer to pick and choose the best of each category (see figure 7). The four 100 mil square chips are then mounted on the same header. Ball-bonded wire connections between chips completes the amplifier. The second choice was to interconnect within and between four adjacent circuits by deposited aluminum and dice the wafer into complete amplifier chips (see Figure 8). The decision of which way to go is made by electrical tests on the wafer after ohmic contacts are alloyed to the crystal.

Fabrication

Our circuits are produced from two types of material. The first type consists of a 20 ohm-cm P-type crystal upon which is grown a 1 mil 2.5 ohm-cm N-type epitaxial layer. The second type is a bulk 2.5 ohm-cm N wafer. We shall deal in this paper with the latter since it has the largest number of process steps.

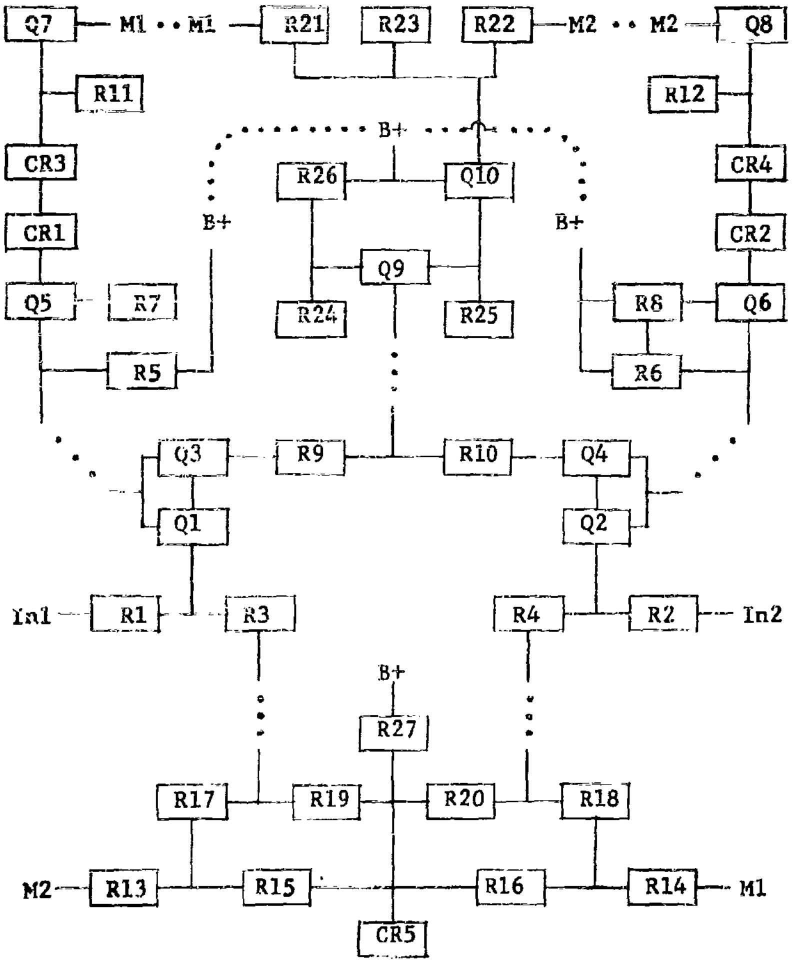

Q7
M1
M1
R21
R23
R22
M2
M2
Q8
R11
R12
B+
CR3
R26
Q10
CR4
B+
B+
CR1
CR2
Q9
Q5
R7
R24
R25
R8
Q6
R5
R6
Q3
R9
R10
Q4
Q1
Q2
In1
R1
R3
R4
R2
In2
B+
R27
R17
R19
R20
R18
M2
R13
R15
R16
R14
M1
CR5

Figure 5

A POSSIBLE ELEMENT CONFIGURATION AS OBTAINED FROM A MORPHOLOGICAL ALGORITHM DEVELOPED AT NORDEN

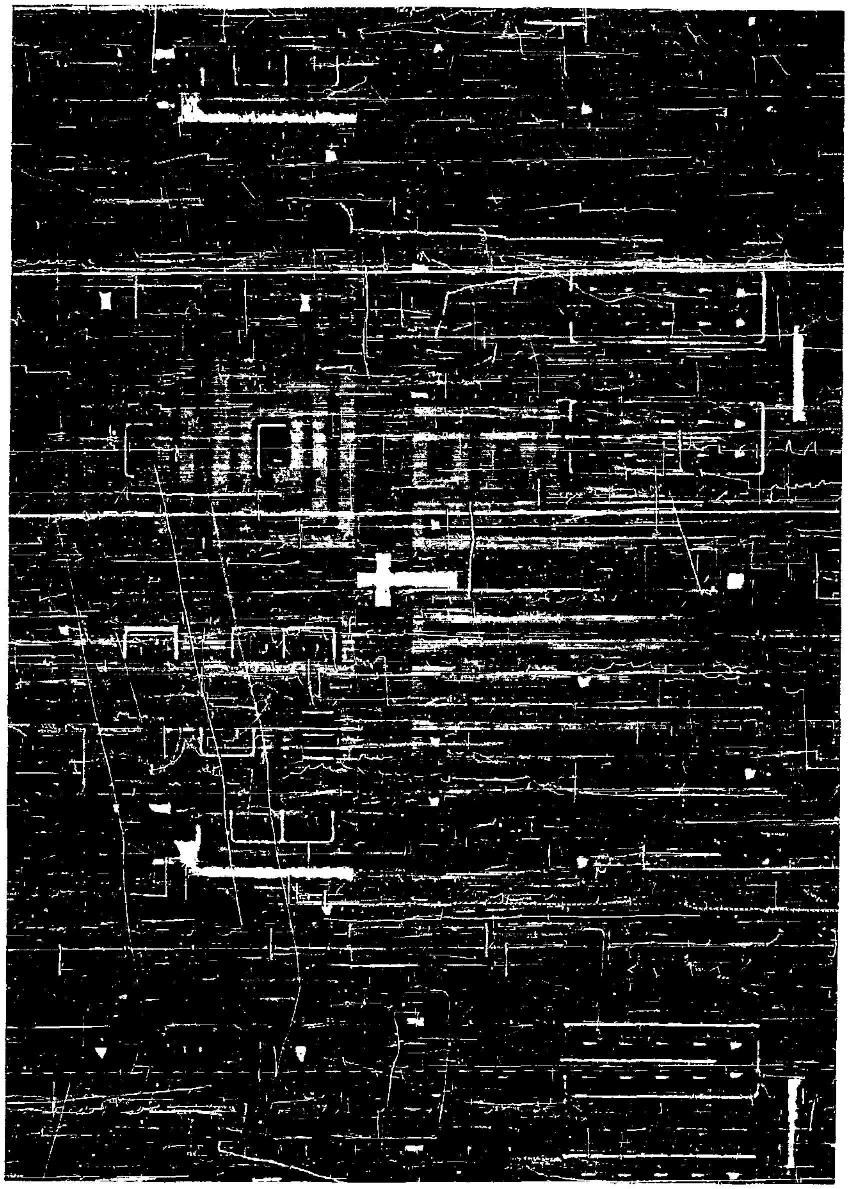


Figure 6
MICROPHOTOGRAPH OF SERVO AMPLIFIER
WITHOUT INTERCONNECTIONS

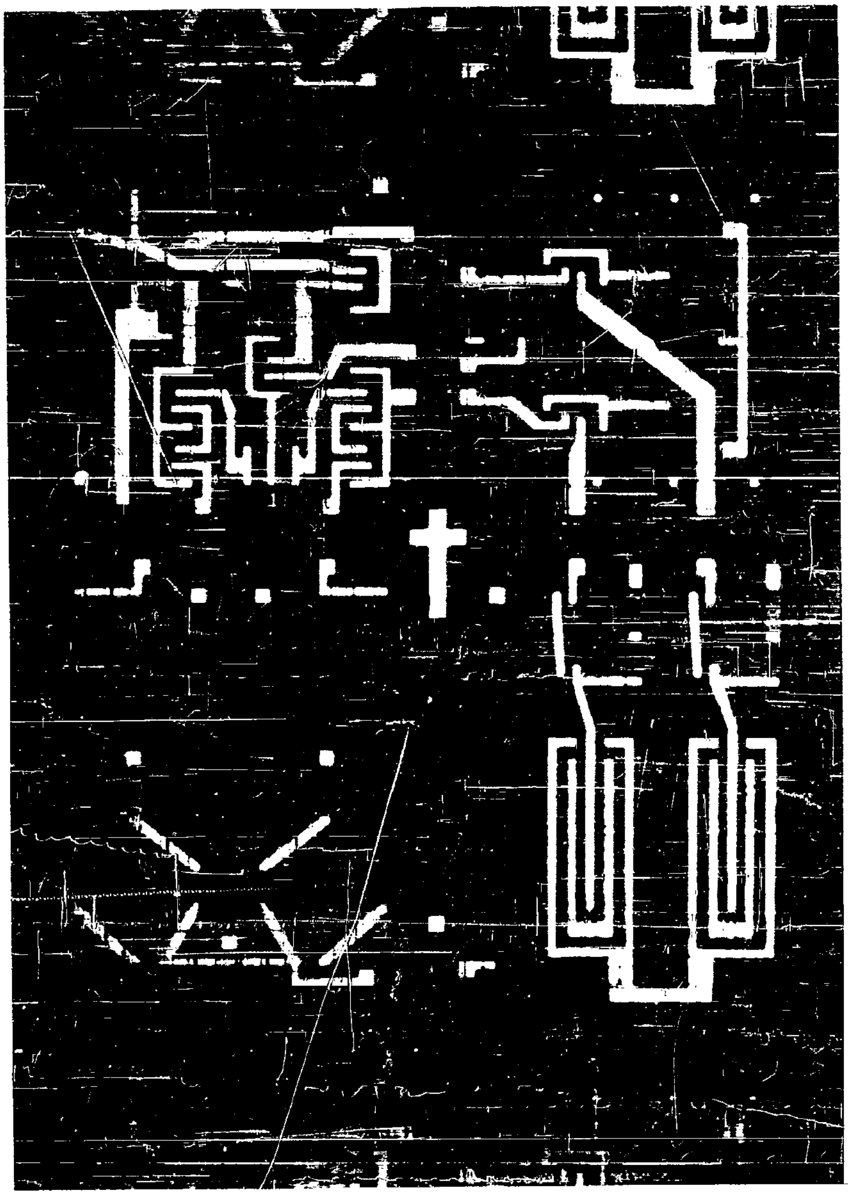


Figure 7

MICROPHOTOGRAPH OF SERVO AMPLIFIER WITH PARTIAL INTERCONNECTIONS

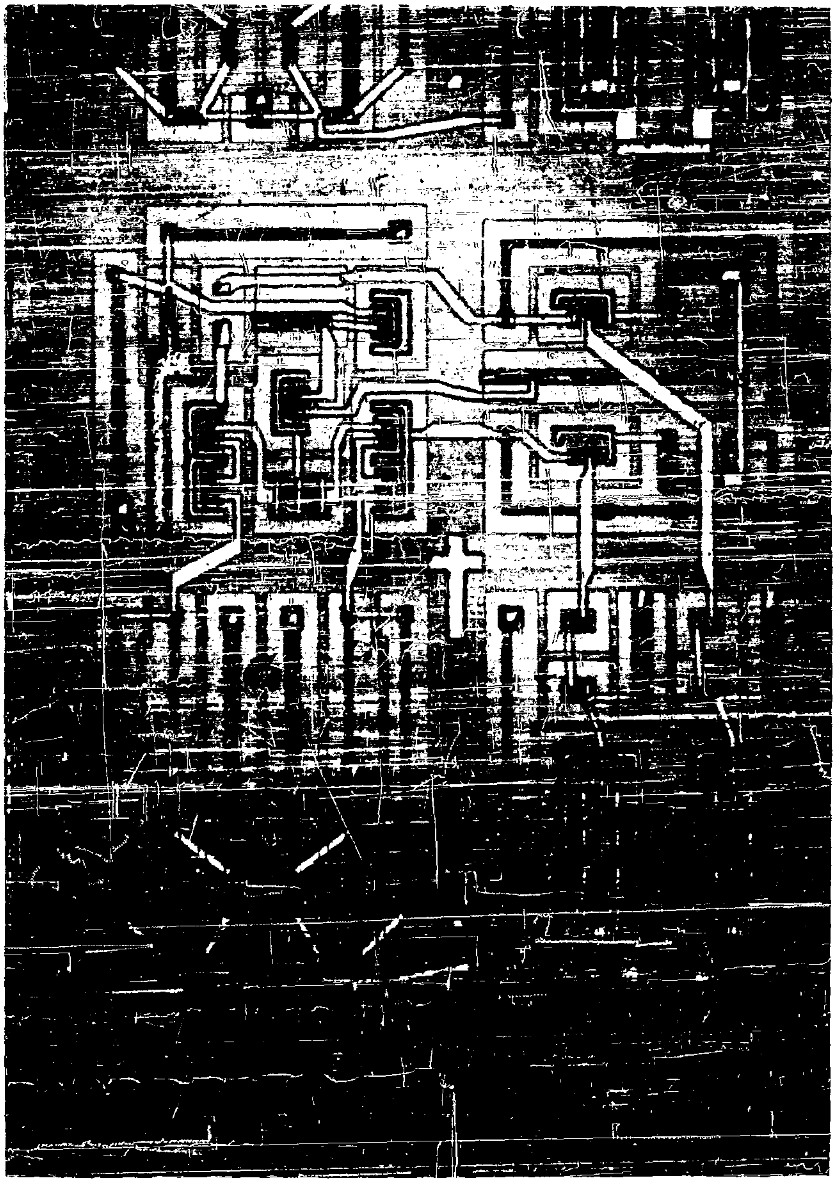


Figure 8

MICROPHOTOGRAPH OF SERVO AMPLIFIER WITH FULL INTERCONNECTIONS

The wafer is lapped and polished to a 4.5 mil thickness. Then 25,000Å of steam oxide is grown and subsequently etched away. This step removes the work damaged crystal layers and yields a smoother surface than mechanical polishing can produce. A 10,000Å oxide is now grown and photoresisted to produce our isolation moat contours. Boron from a tribromide source is deposited (C_o approximately 10^{21} per cm^3) and simultaneously diffused from top and bottom, thus creating N regions which are isolated by back-to-back junction planes. The bases of our transistors, the P part of our diodes, and all resistor networks are now diffused from a Boric acid source. The predeposition is controlled so that a sheet resistivity of 250 ohms per square is maintained. The next step is to diffuse all emitters, make N^+ contact areas in the collector regions, and complete the zeners. A standard phosphorus pentoxide process is employed for our N^+ deposition.

Holes are now etched into the oxide where contact to the crystal is desired. Aluminum is evaporated over the entire wafer and subsequently etched completely off the oxide. The aluminum is spike-alloyed into the crystal. Regrowth of P material in the collector regions are prevented by the N^+ diffusion. Interconnection of elements is accomplished by a similar procedure of deposition and removal. The aluminum leads are vacuum baked at 500°C in order to alloy the aluminum into the surface of the oxide layers.

Careful attention to the porosity of the photoresist is maintained throughout, in order to prevent development of pinholes in the oxide. We monitor the KPR in a crossed Nicol prism arrangement looking for small particles and filaments. The impurities reveal themselves by depolarizing light which they scatter. Our oxides are routinely checked by exposure to chlorine gas at 950°C. Pinhole counts range between 0 and 10 per wafer.

After dicing, mounting, and lead attachment, the circuit is electrically evaluated. The good units are then cleaned in deionized water and vacuum baked for 1 hour at 300°C. Hermetic sealing is accomplished by electron beam welding at Hamilton Standard, Division of United Aircraft Corporation.

Operation of the Amplifier

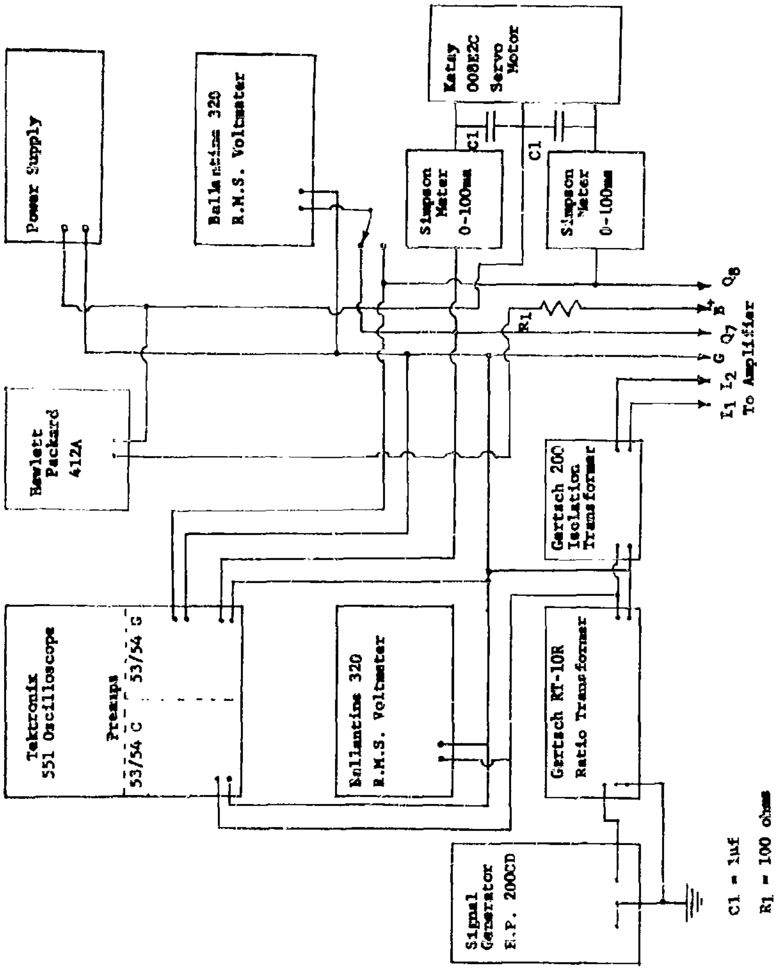
In order to evaluate the servo amplifier functionally, the circuit of Figure 9 is used. A controlled 400 cps input signal is transformer coupled to the amplifier. The input signal is measured both rms and peak to peak. The output of the amplifier is fed into a tuned servo motor, whose primary is open so that the load simulates stalled conditions. The rms output from either Q_7 or Q_8 to ground is then measured. The peak to peak output voltage is measured across the motor windings.

The transfer characteristics of the amplifier is determined by adjusting the ratio transformer and reading input and corresponding output voltages. The rms output is only read across half of the output; however, the two halves are 180° out of phase so that they can be added linearly to obtain the total rms output. Figure 10 is a typical plot of the data. The quiescent current is approximately 60ma per power transistor with an additional 10ma in the B^+ circuit. The current swings between 0 and 120 ma, whilst the rms into the motor winding is 36 volts for a 28 volt supply.

Summary

A 1.5 watt crystal feedback amplifier for servo systems has been developed under BuWeps Contract No. NOw-61-1053-C. Approximately six completed amplifiers are produced simultaneously per 3/4" wafer of single crystal silicon. Each amplifier diffused into the 4 mil thick wafer measures 170 X 170 mil sq. on the surface. Oxide masked planar diffusion techniques were employed throughout, whilst interconnections are of deposited aluminum. The device is a Class A, D.C. coupled A.C. differential amplifier. Being a feedback amplifier the gain is insensitive to internal parameter variation. The following modes of stabilization are employed:

1. Negative Differential A.C. Feedback.
2. Negative Common Mode D.C. Feedback.
3. Negative Thermal Feedback.
4. Thermo-Electric Generation of Stabilizing Potentials.


Power Supply
Ballantine 320 R.M.S. Voltmeter
Ketay 008E2C Servo Motor
C1
C1
Simpson Meter 0-100ma
Simpson Meter 0-100ma
R1
Q_8
E
Q_7
G
I_1 I_2
To Amplifier
Hewlett Packard 412A
Gertsch 200 Isolation Transformer
Tektronix 551 Oscilloscope
Preamps
53/54 G
53/54 G
Ballantine 320 R.M.S. Voltmeter
Gertsch RT-10R Ratio Transformer
Signal Generator H.P. 200CD
C1 = 1uf
R1 = 100 ohms

APPARATUS FOR MEASURING SERVO AMPLIFIER PARAMETERS

Figure 9

APPARATUS FOR MEASURING SERVO AMPLIFIER PARAMETERS

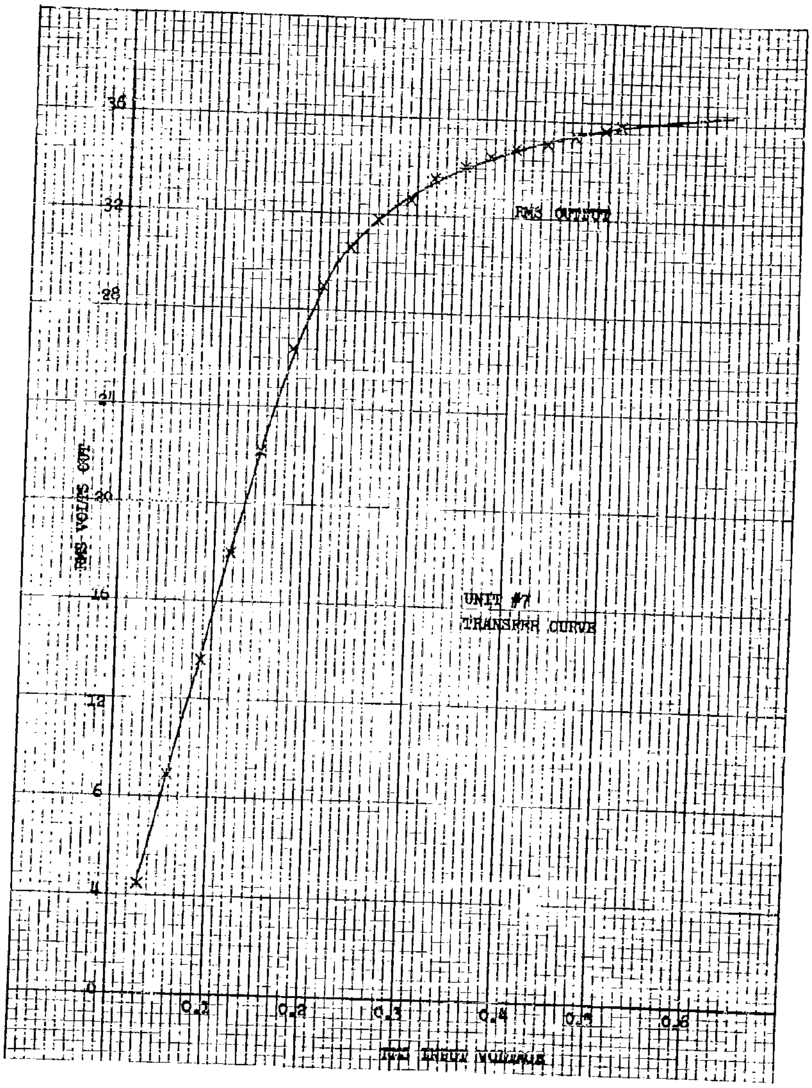


Figure 10
UNIT #7 TRANSFER CURVE

The device contains 10 transistors, 5 diodes and 27 resistors in a single crystal chip, with all circuit interconnections deposited on the passivated surface.

The transistors are capable of sustaining 75 volts during the swing of the 400 cycle signal and deliver up to 200 MA into size 11 and size 8 servo motors. A major contribution to the success of this project was topological inversion of the output transistors, to obtain extremely low saturation resistances. All contacts are made to the top surface.

A family of amplifiers up to 25 watts can be obtained by varying the output stage design and heat sink configuration of the header case.

This paper represents the work of a small but dedicated team of scientists and engineers at Norden, who have been generously supported by United Aircraft Corporation and the Navy Bureau of Weapons under contract No. NOw 61-1053-C. The author wishes to express his gratitude to all, and in particular, Mr. F. J. Hierholzer, Mr. R. Lovelace, Mr. W. Salmre, and Miss P. H. Jeffrey.

A STATUS REPORT ON INTEGRATED CIRCUITS

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Phoenix, Arizona

It is my assignment today to give a status report on integrated circuits from the component manufacturer's point of view -- with some sort of prediction into the future of what we shall be able to do and on what time scale.

This is of course a difficult job for many reasons. In fact it is really an impossible job to do accurately since it would require me to predict inventions that have not yet been made.

One can compare the era of vacuum tube technology with the era of transistor technology in order to see how our time scale has compressed.

It is difficult to specify when vacuum tube technology was first demonstrated in the scientific laboratory in a way that could compare with the first demonstration of transistor action by Bardeen Brattain and Shockley. The Edison effect was demonstrated in 1883, but the triode or grid action was not demonstrated until 1907 by DeForest. Let us take 1907 then as the beginning of the era of vacuum tube technology and let us take 1957 as the essential end of this era for our purposes, neglecting of course, special purpose applications which promise to offer incentive for many years to come to those of us in the solid state industry.

The development of vacuum tube technology and circuitry during this fifty year period was extremely slow by our standards today. By comparison, the transistor has been with us for 14 years.

I have been invited to discuss the proximity of the demise of the transistor. If we were to call upon our past experience in order to make these predictions, I fear we would be overly cautious. I personally believe that most people who have had the courage to go on public record in order to make such predictions have been too chary.

We need not regress to the time of Fleming and DeForest to compare the pace of technology then with our technology today in order to give us proper perspective, but need only go back to the spring of 1954 at the NAEC in Dayton, Ohio. I had the pleasure of being at that meeting and attended a gathering devoted to silicon transistors much as this meeting today is being devoted to integrated circuits. I would say that the level of our general competence in producing silicon transistors then was certainly no better than our ability to produce integrated circuits today.

I sat through several papers in that session discussing the progress to date given by some of the outstanding laboratories in this country then and now. It was the consensus of all the speakers that many problems remained to be solved in silicon technology and in the application of silicon devices. Circuit and systems engineers could not hope to have even early developmental samples for an estimated 3 to 5 years minimum.

The last paper at that session was given by my good friend, Gordon Teal, in which he announced that Texas Instruments was in mass production of these much-wanted silicon transistors. To be sure, the characteristics of those early devices were poor and I would venture a guess that the yields even to some rather sloppy sets of characteristics, were not high, but all of you know the rest of the story.

It appears that even as late as 1954 very few people in the United States had the vision to predict accurately the timetable for the adoption of silicon transistors, or they lacked the courage to back their vision with the necessary investment of people, facilities and capital.

I hope these examples have paved the way for me to make the predictions which are always expected of keynote speakers. My prediction is that the era of integrated circuits is here. To be sure, we have many problems facing us. Our yields are too low and hence our costs are too high. We need many circuit and device inventions to bring the era into full bloom, but the era of integrated circuits is with us today as surely as the era of silicon transistors was with us in 1955. There is one addition that should be made to this prediction. That is the fact that the rate of advance of our technology has nearly doubled since 1954. Hence, I would expect as a minimum that if one looks at the growth of unit volume of integrated circuits over the next few years, he would have to at least double what happened in silicon transistors in order to find an approximate base to use for the advent of these new and advanced circuits. It is probably valid to double the figures since both sets of numbers are limited by the capability of our technology to produce and apply these sophisticated devices and have not in the case of silicon, and will not for at least 5 - 7 years in the case of integrated circuits, be limited by the ability of our technology to use these devices.

Now I have made my prediction and I hope part of what I have to say will justify my optimism. However, I am certain there is another area in which you would like a prediction. That is the precise direction which integrated circuit development will take during the next decade. Here I feel I am justified in being a little vague. It is one thing to evaluate known methods and techniques and another to try to predict the unknown. I feel certain that ten years from today the most advanced integrated circuits will be made by processes not yet in common use and might possibly use phenomena and materials not yet discussed in any meeting on integrated circuits.

The ultimate goal of integrated circuits is, I believe, to be able to construct on a molecular basis a piece of material that will in itself perform the function desired. It, hence, would not be considered an integrated circuit or even a complex device by our normal definitions of these terms today. I have noted that since Townes and Bloembergen have shown us how to build entire microwave or light amplifiers out of a solid hunk of simple material, such as ruby, we don't refer to these entire amplifiers as integrated circuits but as basic devices in the same class as a thermistor or a diode, and hence less complex than a transistor. I don't argue with the definition. I only point out that our ultimate goal is to reduce all circuit functions to such basic devices. Our ultimate goal then is to greatly reduce the complexity of electronics rather than to increase it. Obviously, many inventions of the caliber made by Townes and Bloembergen are needed before we can achieve this goal in any appreciable percentage of the circuits and functions we find necessary to build our electronic equipment. It is not for me, today, to peer into a crystal ball and predict what will come to pass or when. However, I shall predict that some of these inventions will be made in the next decade.

It is, I believe, more fitting for us to evaluate the various methods which are being used, and to see which approaches offer the greatest potential for the time being.

Impact of Microminiaturization on Digital Circuits and Computer Systems

The evolution towards microminiaturization has essentially taken place from the time the field of electronics was born some fifty years ago. From the earliest radios to today's computer systems, we have seen components become smaller and more reliable, packaging techniques have evolved from primitive forms of chassis mounting to printed circuit boards, from printed circuit boards to modular packaging, and finally and perhaps most important; the cost, size and weights of these systems have been reduced by several orders of magnitude. However, it should not be implied that the reduction of cost and size have been the only motivating factors. Because today's systems have grown so fantastically complex, composed of increasingly large numbers of components, the reliability of these systems has become increasingly important despite the fact that individual components are being produced to more stringent reliability standards; this greater component reliability has not off-set the augmented probability of system breakdown. Various forms of microminiaturization promises greater inherent reliability, but to achieve this promise a research and engineering development program is necessary. The electronics industry is now engaged in this program.

Over the last five years microminiaturization has taken many forms; almost as many forms as there are companies engaged in this work. Naturally, as in any new field, clear lines of directions are not yet fully evident. Concepts have not yet fully crystallized and considerable effort goes into inventing trade names, often as not for products not yet fully developed, which tended to create confusion in the early stages of microminiaturization. The approaches developed so far may conveniently be divided into the three following categories:

1. The component oriented approach which includes tighter packaging techniques using conventional components and miniaturization of hardware accessories. These approaches represent relatively modest extensions of the state-of-the-art. Examples of this approach are the RCA micromodule, the pellet approach, G. E.'s Timm packages, etc.

2. The Circuit Oriented Approach

In this approach we have substrates containing circuits and sub-circuits with usually a one-to-one correspondence between circuit diagrams and substrate elements. Thin film and separate chip circuits constitute examples of this approach.

3. Function Oriented Approach

These represent approaches in which a single piece of semiconductor material is altered to obtain the desired functions. This approach is also known as the single chip approach, or as an integrated circuit, or FEB.

Since the circuit oriented and the function oriented approach are the ones that are most vigorously investigated at the present, and since these approaches probably have the greatest potential for the immediate future, I will limit my discussion today to these approaches.

First, let us look at the techniques by which we construct some of these advanced FEB.

The fabrication of a special single chip, or "FEB", requires a "mask set". These "mask sets" are neither cheap nor easily changed. On the other hand, they offer the best promise of

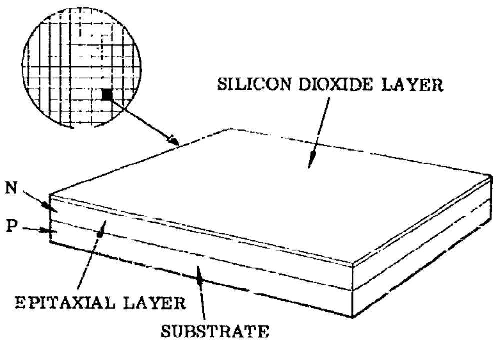

SILICON DIOXIDE LAYER
N
P
EPITAXIAL LAYER
SUBSTRATE

Figure 1 - Initial Wafer Processing

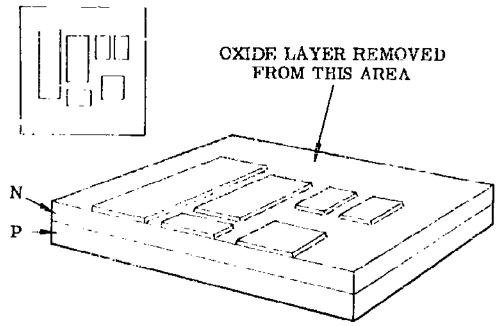

OXIDE LAYER REMOVED FROM THIS AREA
N
P

Figure 2 - Selective Etching

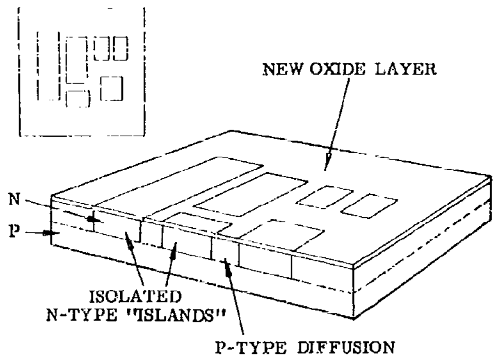

NEW OXIDE LAYER
N
P
ISOLATED N-TYPE "ISLANDS"
P-TYPE DIFFUSION

Figure 3 - Isolation Diffusion

highest reliability at lowest long term cost. Since integrated circuit mask set design is perhaps unfamiliar to most electronic engineers, a review of this area, as well as how the mask set is used to fabricate circuits, might be helpful.

The mask set will form the transistors, diodes, resistors, capacitors, as well as the necessary circuit interconnections. The mask is accurately drawn to a large (200:1) scale. Mask layout requires a complete understanding of the process to be used, as well as knowing the significance of tolerances and parasitics and their effect on circuit performance. After photographing the mask, images are multiplied and reduced to final size. Six to eight masks are often required to perform all the processing steps. If adjustments are required in the final circuit, this entire costly process must be repeated.

As an example of the fabrication procedure for functional electronic blocks, let's consider some of the steps in making a particular logic circuit, in this case a NAND-NOR circuit. Figure 1 shows an enlarged portion of a silicon wafer. The wafer itself will accomodate many dozens of identical circuits but, for our purposes, let's follow the processing of the area required for only one circuit. The first processing step is the growth of an epitaxial N-type layer on the initial P-type substrate. A protective oxide layer is then deposited over the epitaxial layer.

The first masking process, in Figure 2, consists of electrically isolating the areas in which the circuit components will be formed. This is accomplished by the selective removal of the oxide coating by means of a mask leaving isolated "islands" of oxide over the "component" areas. As shown in Figure 3, the second step is to diffuse a P-type material into the exposed epitaxial N region, so that all "islands" are surrounded by P-type areas. Since the islands are N-type regions, it will be noted that there exists an NP-PN junction between any two "component islands". These junctions, in effect, represent back-to-back, reversed-biased diodes which are so far apart that no transistor action occurs. As a result, there exists a high resistivity area between all components on the substrate. The "islands" in themselves represent the collector regions of transistors, or they can be used for the deposition of other integrated circuit "components". At the end of the diffusion process, a new layer of protective oxide is grown over the previously exposed area.

Next, a mask of the transistor base regions, the anode portions of diodes and junction capacitors, and various resistors is placed over the wafer and windows are etched through the oxide layer at the exact locations where these components are to be formed, Figure 4. A P-type diffusion then forms the desired components within these "exposed" areas, and another protective oxide layer is grown, as shown in Figure 5.

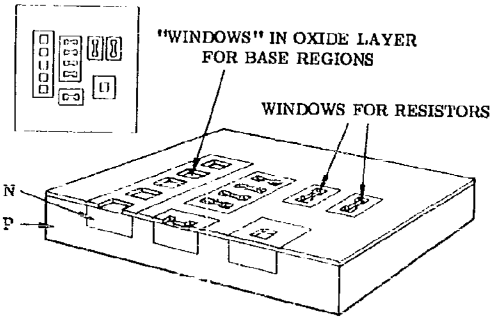

"WINDOWS" IN OXIDE LAYER
FOR BASE REGIONS
WINDOWS FOR RESISTORS
N
P

Figure 4 - Selective Etching
For "Components"

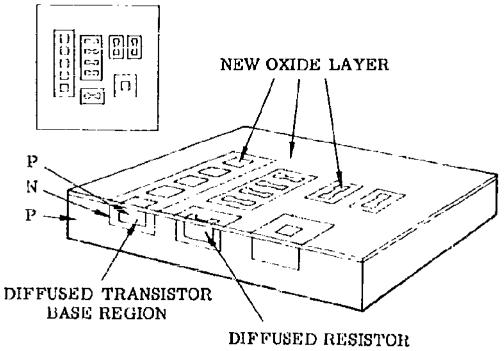

NEW OXIDE LAYER
P
N
P
DIFFUSED TRANSISTOR
BASE REGION
DIFFUSED RESISTOR

Figure 5 - First "Component"
Diffusion

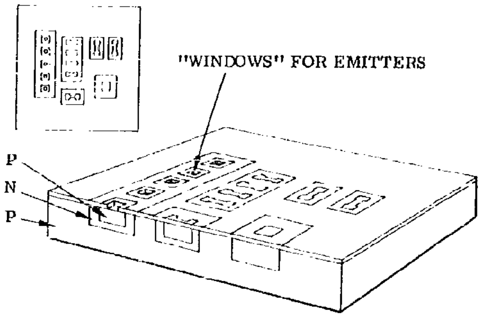

"WINDOWS" FOR EMITTERS
P
N
P

Figure 6 - Second "Component"
Etching Process for Subsequent
Diffusion

In the next step, Figure 6, another mask is placed over the wafer corresponding to the transistor emitter regions, the cathodes of diodes, and other areas needed to complete the partially formed components of the previous steps. A third diffusion process then completes the manufacture of the individual components and, again, an oxide layer is formed.

In final masking steps, the oxide is selectively removed to permit the metallization process for the interconnecting pattern between the various parts to be completed, as shown in the final photograph of Figure 7.

It must be remembered that the foregoing operations are performed simultaneously on dozens of circuits on a wafer. After completion of the final pattern, the wafer is diced -- that is, cut apart into individual circuits -- and each circuit is individually packaged.

I've briefly covered the fabrication procedure of integrated circuits primarily to emphasize one point: The same procedural steps and processes used for making a single transistor are used for making a complete integrated circuit -- and the complete circuit, in fact dozens of circuits, are made virtually in the time it takes to make a single transistor. Resistors, for example, are made concurrently with transistor bases and all portions of the complete circuit are finished at the same time as the transistor emitter. The cost of fabrication, therefore, assuming no losses, is extremely reasonable. A wafer of 66 integrated circuits costs from $10.00 to $20.00 ... an individual circuit is only 20 to 25 cents. Packaging and testing however would at least double this figure.

At this point, the major implication of integrated circuits is clear: it is, very simply, the economic advantage of integrated circuits compared to the circuit elements they will replace.

We have omitted the most important single cost factor: yield. If only one of the 66 circuits is good, the cost varies from ten to twenty dollars each. Yield then becomes the chief profit determining element in the competitive market place. Yield is, of course, affected by complexity, tolerances, and circuit design, as well as by the performance expected of the finished unit. Thus, the company who is likely to be the most successful in the long run is the one with the most highly developed technology. A background in the production of large quantities of silicon planar epitaxial transistors is extremely helpful. It is difficult for outsiders to enter the market place without people trained in the art and without many millions of dollars of equipment required for economical production.

We have just gone through the steps for producing a FEB. From this one might assume it is a relatively easy task and that

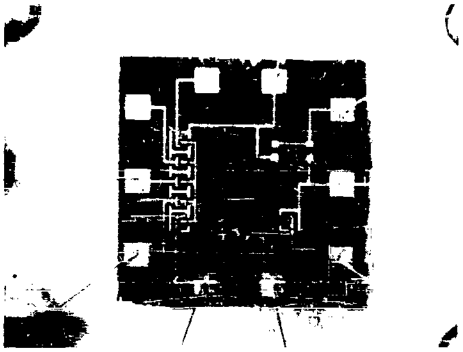


Figure 7 - Photo of Final Device Shows Metallized Interconnecting Pattern

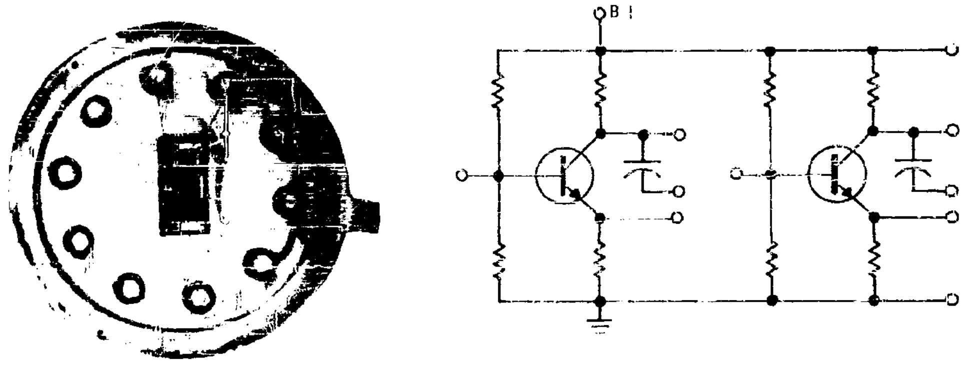


Figure 8 - Schematic Diagram and Equivalent Device of Universal Linear Amplifier

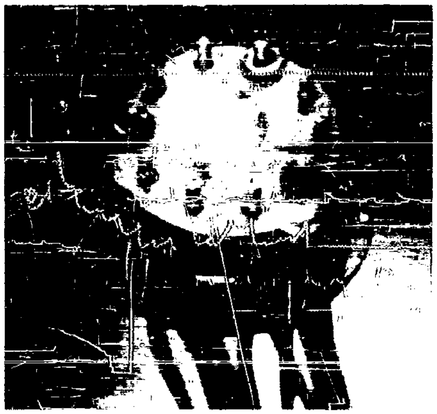


Figure 9 - Header-Mounted Amplifier Has By-Pass Capacitors Separately Mounted Below Ceramic Wafer

now we are ready to take over all electronic subassembly.

Actually, this is not the case. We have discussed, so far, only the construction of a logic circuit for a digital computer and this is the ideal area in which we can impress the world with our know-how.

First, logic circuits are infinitely easier to build by these techniques than are linear circuits. The linear circuit engineer is concerned with gain, frequency distortion, intermodulation distortion, noise figure, ability to AGC, etc.

To build the required characteristics for such circuits simultaneously into a single block of silicon is far more difficult.

In addition, if one can come up with a better logic circuit and get it designed into a computer, there is a good chance one might sell millions of the identical circuit.

Such large unit volume allows one to spread the engineering overhead of design and alterations, and the costly mask making operations, over a large number of units so that the cost charged to each unit is trivial.

However, such large individual markets do not exist for linear amplifiers. Hence, the economics of the situation indicate that other approaches to this problem must be thoroughly evaluated.

An example of what one encounters in this area is demonstrated by a universal linear amplifier we have recently developed for the Air Force.

Figure 8 shows the schematic diagram and the equivalent FEB circuit. This, however, is only a basic circuit since, in addition, bypass capacitors are required to optimize the performance for a particular frequency range. These capacitors are not built into the FEB, but can be added separately. Figure 9 shows a device in which the basic amplifier is built on one wafer with two capacitors deposited on the header beneath. Figure 10 shows a single capacitor mounted on the same wafer with the basic amplifier.

The cost of the two bypass capacitors completely overshadows the cost of the amplifier without bypass. From pure economics, therefore, one is forced to attempt to find a better way.

In addition, most amplifiers end up being more complex than this particular one. To attempt to put these complex amplifiers on a single block of silicon is foolhardy at our present stage of technology.

Figure 10 - Same Amplifier With Single Capacitor Mounted on Same Wafer

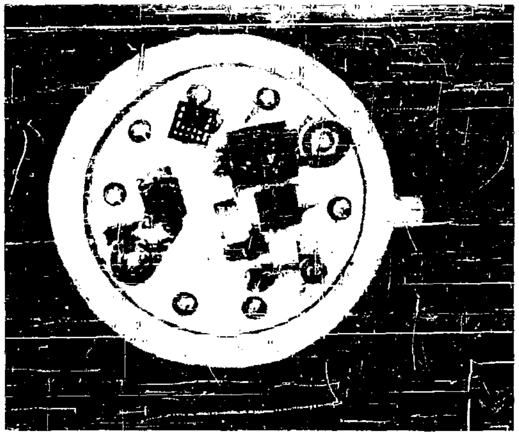
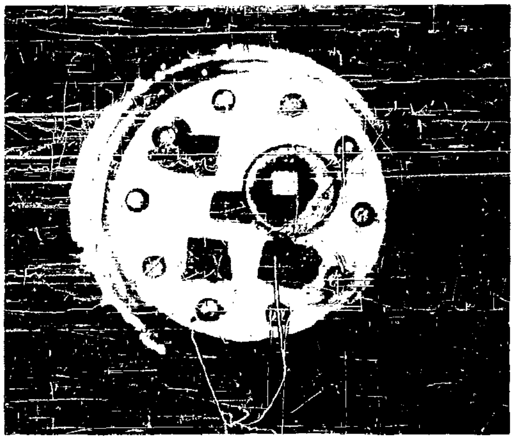


Figure 11 - Hybrid Audo Amplifier Utilizes FEB Darlington Circuit

Figure 12 - Typical Example of Hybrid I-F Amplifier



While it certainly can be done, the cost would be prohibitive unless someone had a requirement for hundreds of thousands of identical circuits in order to spread the tremendous overhead design costs and learning costs to a reasonable basis.

It is much more reasonable today to go back and look at some of the thin film approaches to integrated circuits for these applications.

An example of what one runs into is shown in Figures 11 and 12 which depict an audio amplifier using Darlington FEB and a hybrid IF amplifier, respectively.

These are examples of one practical approach. I personally do not think it is optimum, but these circuits can be constructed very cheaply (perhaps at a cost of 1/100 of a FEB, even at good yields) and they can be constructed and put in operation in a matter of 1 or 2 days instead of 2 or 3 months.

Actually, as yet we have not found the proper solution for the ideal integration of custom-built circuits which will be used in low volume and which today require the fantastic characteristics demanded by linear circuit designers.

For linear devices, I feel the best solution at the present is a combination of the hybrid techniques just illustrated, together with evaporated or sputtered thin films.

Here is a field where we definitely need invention. We need clever circuit inventions to help us eliminate large capacitors and large inductors, and we need processing inventions that will let us construct these circuits with the same performance and flexibility we have today at approximately the same cost.

Let us now go back and examine more closely our status in the one area that offers the greatest immediate promise of payoff.

Before we delve into the details it might be worthwhile to look at a series of photographs that show our sophistication today in these various fields. (See Figures 13 through 19)

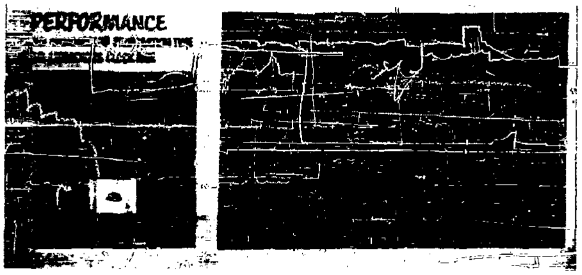
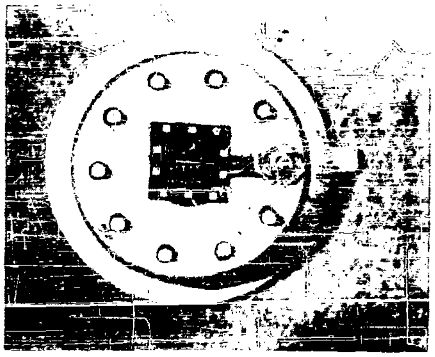


Figure 13 - Poster of NAND-NOR Logic Circuit

Figure 14 - Enlarged View of Header Mounted Logic Circuit



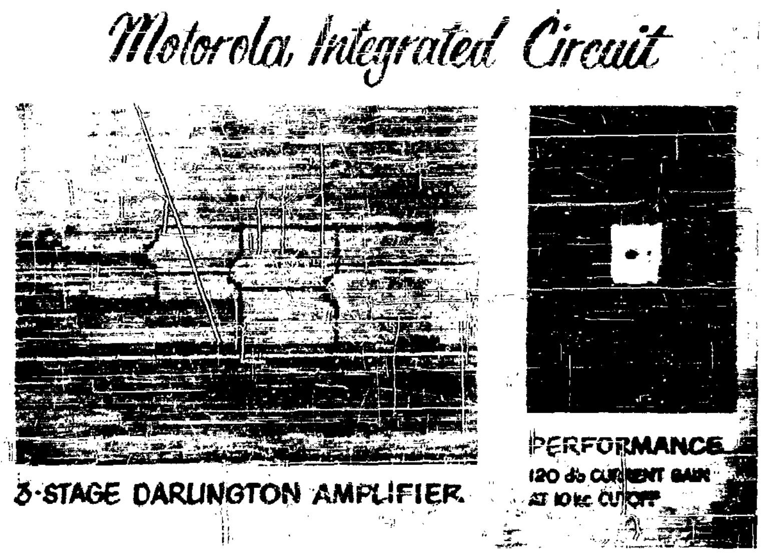

Motorola Integrated Circuit
3-STAGE DARLINGTON AMPLIFIER
PERFORMANCE
120 db CURRENT GAIN
AT 10kc CUTOFF

Figure 15 - Poster of Integrated Darlington Amplifier Circuit

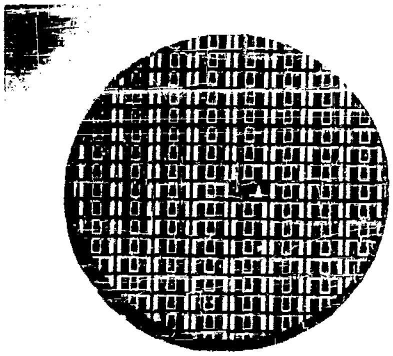


Figure 16 - Wafer of FEB High-Frequency Amplifiers

There are many others, but I feel this selection of devices, circuits and equipments will indicate clearly that this era of integrated circuits is now ready for application in many fields of endeavor.

Where do we stand now in the design of computers by these techniques?

Impact of Microminiaturization on the Design of Logic Circuits

The design of logic circuits involves a compromise between many conflicting requirements. For circuits built of conventional, discrete components, these requirements may be summarized as follows:

1. The circuit must be reliable, which means that it must be insensitive to variations in components values due to temperature and aging. Also, in order to be able to produce these circuits with a reasonable yield, the required tolerance requirements on the components should be as large as possible.

2. A logic circuit must have sufficient logical capability. This means that the circuit must perform a Boolean operation from which all necessary logical functions can be realized.

3. The propagation time through the logic circuit should be as small as possible with power dissipation kept at a minimum.

4. The noise immunity of the logic circuit should be large so that noise signals appearing at its various inputs will not result in erroneous operation.

5. Fan-in and fan-out capability should be as large as possible.

6. A logic circuit should have good interconnection capability which means that "no signal carrying inputs", such as necessary power supplies and biases, should be kept at a minimum. Also, the interconnection problem is generally eased if the basic building blocks are capable of performing a number of logic operations simultaneously and if the logic function performed is more complex.

When a logic circuit is integrated, some additional requirements are imposed due to a number of conditions peculiar to the

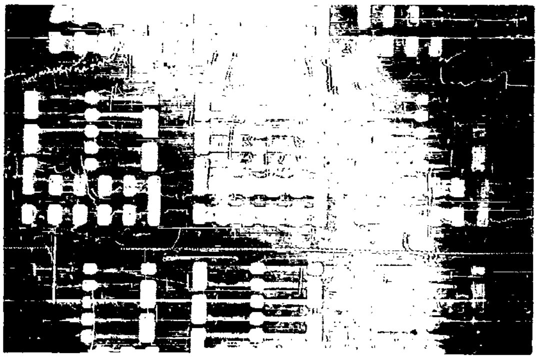


Figure 17 - Typical Multi-Tapped Resistor Configurations

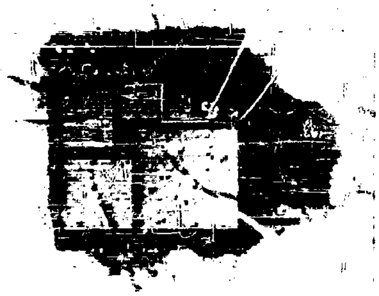


Figure 18 - Typical Binary Capacitor Configuration

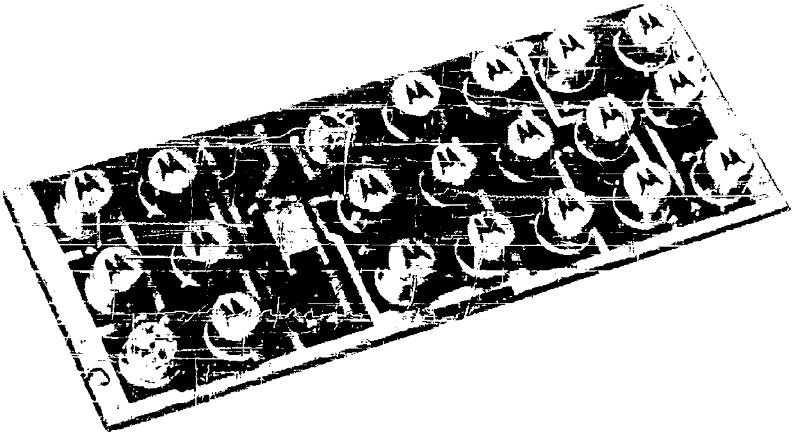


Figure 19 - 120-Mc Transceiver Prototype

device processes. First, parasitic coupling between various parts of the circuit is introduced through the substrate. Second, certain elements or certain ranges of components values cannot be easily realized by present day techniques. A typical example of this latter limitation is inductances for which values above 1 microhenry are difficult to realize. Also, since the inductance had to be topilogically laid out in a plane, the maximum Q obtainable is about three.

To see how these limitations affect the operation and design of logic circuits, let us use as an example the diode - transistor NAND circuit shown in Figure 20. The diodes at the very left in this slide represent the input diodes and perform, together with the 1K resistor, the logical "AND" function. The two diodes connecting the 1K resistor to the base of the transistor are respectively an "OR" diode and a bias offset diode. The base of the transistor is connected down to a negative power supply in order to make the transistor turn off rapidly. The output from the circuit is taken from the collector of the transistor. In this circuit, a logical zero and a logical one are represented by a high positive voltage and a low positive voltage (nearly ground potential) respectively. Therefore, if none, or one, or two of the inputs has a logical zero applied to it, the current through the 1K resistor from the +6 volt power supply will flow to ground through whatever diodes are connected to the logical zero. The transistor therefore remains cut off and the collector is at the high positive potential representing a logical one at the output. However, if all the inputs have a logical one connected to them, all the "AND" diodes will be cut off and the current through the 1K resistor will therefore flow into the base of the transistor and turn it on. The collector will subsequently be at a low potential and the output will therefore register a logical zero. In other words, the circuit performs the "NAND" logical function which means not A, not B, not C.

Figure 21 shows how this circuit would be made on a common substrate. Since NPN transistors are used, the substrate is of the P-type so that the collector of the transistor will not be shorted to the substrate. The realization of the three "AND" diodes are shown at the very left. Since these diodes have their positive terminals connected together; that is, the P part of the respective junction connected together, N-type material had to be diffused into the substrate for the purpose of isolation. After that, P-type material is diffused into the N and then three small N diffusions are performed to create the negative terminals of the diodes. In other words, instead of three diodes, we have, in fact, made a transistor with three emitters. However, transistor action is at this point undesirable so the collector and base are shorted together during the metallization operation.

Located next to the "AND" diodes are, respectively, the 1K resistor, the 5K resistor and the 400 ohm collector load resistor.

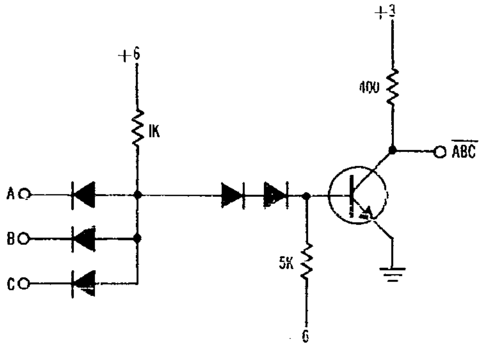

+3
+6
400
IK
$\overline{ABC}$
A
B
C
5K
6

Figure 20 - Diode-Transistor Logic Circuit

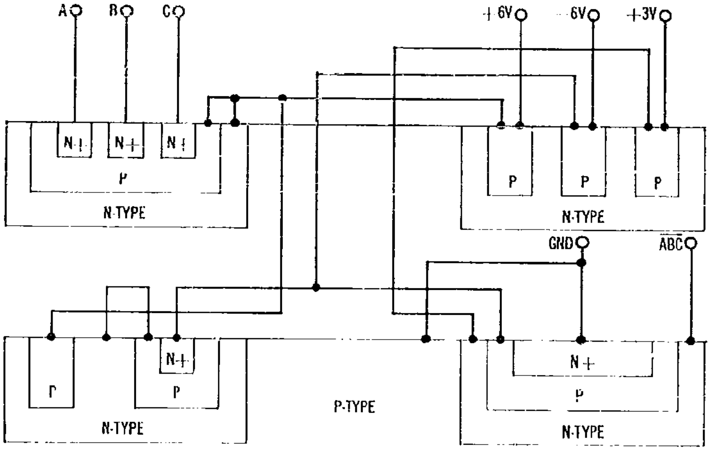
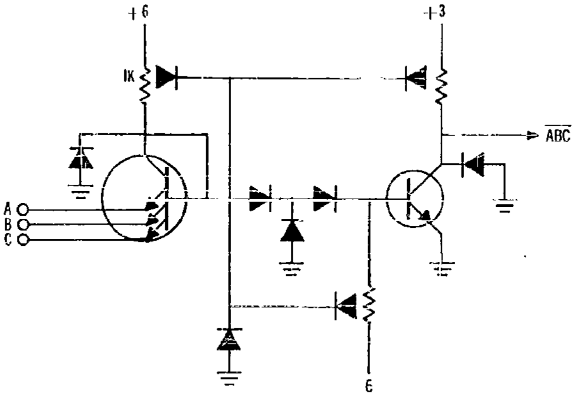

A
B
C
+6V
6V
+3V
N+
N+
N+
P
N-TYPE
P
P
P
N-TYPE
GND
$\overline{ABC}$
N+
P
P
N-TYPE
P-TYPE
N+
P
N-TYPE

Figure 21 - Diffusion Diagram-DTL Gate


+6
+3
IK
$\overline{ABC}$
A
B
C
6

NOTE: With each diode shown there is an associated capacitance which is proportional to Area and inversely proportional to reverse voltage.

Figure 22 - Fully Integrated Diode-Transistor Logic Circuit with Accompanying Parasitics

Again, N-type material is diffused into this substrate to provide isolation and the resistors are obtained by utilizing the resistance across a long strip of P material diffused into the N-type material. In other words, the resistors are really stretched out backward, biased diodes with a resistance created between the two ends of the P-type material. The "OR" and the offset diodes are made the same way as the "AND" diodes and the transistor is realized in the conventional way.

Figure 22 shows the equivalent circuits for the integrated logic circuits. As mentioned before, the cluster of input "AND" diodes is now a multiple emitter transistor with its collector shorted to its base. The diode down to ground in its collector represents the coupling to the substrate, which is here assumed to be grounded. Also, since all the resistors are constructed out of backward diodes with common N-type material, these are also coupled to the substrate through a diode. Because of the junction capacitance of the diodes, capacity coupling now exists from the collector back to the base through the 1K and 5K resistors. In other words, the process of integration has created additional "Miller effect" type coupling between collector of transistor which will tend to slow down the operation of the circuit. This is demonstrated in Figure 23 which compares the transient response of a discrete "NAND" circuit with that of an integrated one.

Finally, because components cannot be selected in an integrated circuit, parameters and individual elements will have much larger tolerances than their discrete counterparts. For instance, it is not unusual that the beta may vary as much as ± 100% from one transistor to the next and it is difficult, if not impossible, at the present, to make integrated resistors with tolerances less than ± 20%.

The design of an integrated logic circuit is therefore a more difficult task than the design of its discrete component counterpart. However, to partially counteract the detrimental effects introduced by the device limitations, there are certain circuit design procedures to which one can resort. For instance, to counteract the effect of parasitic coupling through the substrate, the circuit should be designed so that the node at which all logical connections are made has as low an impedance level with respect to ground as possible. An integrated logic circuit should incorporate some kind of feedback or compensation so it can tolerate the large tolerance limits of integrated components. Moreover, since semiconductor components vary in an exponential fashion with temperature, some kind of temperature compensation should also be incorporated. Finally, to take full advantage of the space saving capability of integrated circuits, the interconnection of logic circuits will probably also eventually be microminiaturized. This means that connections furnishing, for example, the power to the logic units will contain some amount of resistance resulting in lowered regulation of power supply voltages. Henceforth, integrated logic circuit must be more insensitive to variation of power supply voltages than its discrete counterpart. In other words, the integrated logic block should incorporate some means for tracking the power supply. Finally, microminiaturized interconnecting and packaging will lead to greater mutual capacitance between adjacent connections resulting in an overall higher cross-talk and noise level. Hence, the requirement for noise immunity is more stringent in an integrated circuit.

A circuit that circumvents most of the detrimental effects peculiar to integration is shown in Figure 24. It consists essentially of an NPN current mode switch with emitter followers coupling the signal from the collectors of the gate to the output. The current switch in turn contains six transistors, five of which have their bases connected to the respective inputs. The base of the sixth transistor is connected to a fixed bias such that this transistor is conducting when no signal is supplied to any of the inputs. The circuit has two emitter follower coupled outputs; one taken from the collector of the fixed bias transistor and the other from the common junction of the collectors of the five input transistors. The emitter follower serves a two-fold purpose in this gate. First, it serves as a DC translator so that the DC level at the outputs of the gate is compatible with the level requirements at the various inputs. Secondly, since the emitter follower has a low output impedance it provides the gate with a large fan out capability.

If a positive signal representing a logical "1" is applied to any of the inputs, the collector of the fixed bias transistor goes positive and the output from the common collector output goes negative. The two outputs, therefore, perform the logical operations "OR" and "NOR", respectively. If, on the other hand, a negative signal had been used to represent a logical "1", the basic gate would, of course, perform the logical operations "AND" and "NAND".

This type of circuit is extremely reliable and highly insensitive to variations in component values, parameter changes and power supply drifts. This is due to the large amount of feedback furnished by the common emitter resistor and the DC translating characteristics which are not dependent upon the actual values of the resistors in the circuit but only upon the ratio between them.

The fan-in and fan-out capability of the circuit is large because of the low impedance level of the common emitter node and because of the inherent high input impedance due to the feedback action of the common emitter resistor.

Its logical capability is high because it performs the "OR-NOR" logical functions simultaneously and because of its large fan-in, fan-out capability.

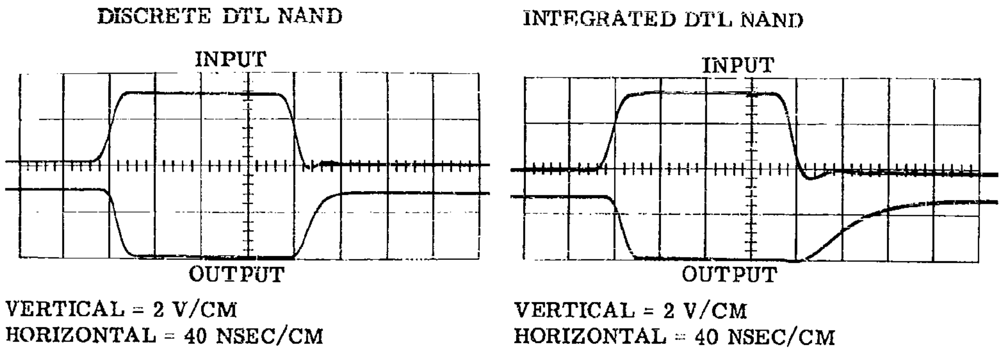


Figure 23 - Transient Response of Discrete and Integrated DTL NAND Circuits

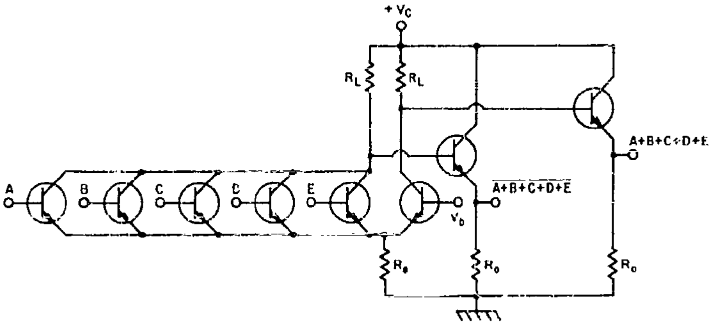

+Vc
RL
RL
A
B
C
D
E
A+B+C+D+E
A+B+C+D+E
Vb
Re
Ro
Ro

Figure 24 - Basic Motorola Integrated Gate Circuit

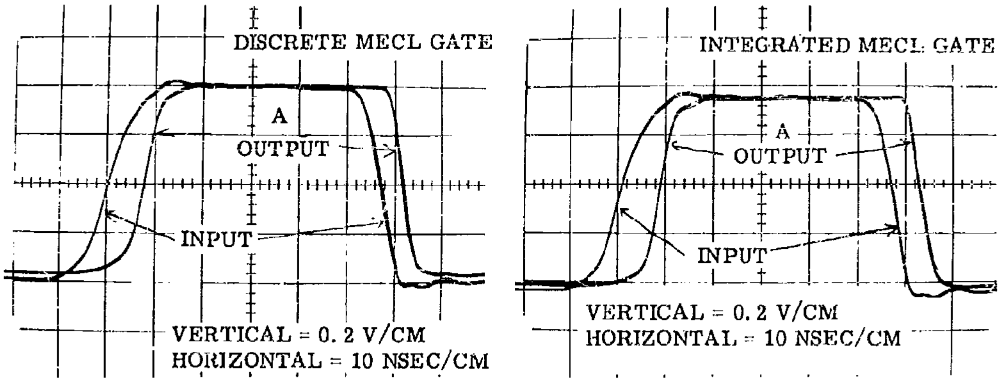


Figure 25 - Performance Comparison of Discrete and Integrated Gate Circuits

The current logic circuit is extremely fast, that is, the propagation delay is very small because:

a) Most of the logic decisions are performed at the low impedance level of the common emitter node.

b) The signal path is through an emitter follower and a grounded base stage, both of which are inherently fast.

c) The transistors in the logic circuit never become saturated.

The circuit has a large noise immunity because:

a) The input impedance of the circuit is high so that only a small amount of current is transmitted from one circuit to the other.

b) The output impedance is low so cross-talk between adjacent interconnections is minimized.

c) Noise generated in grounds and power supply lines is practically nonexistent since the current demand of the MECL blocks is constant independent of state.

Because the tolerance requirements of the circuit are lax, logic blocks of large complexity may be built with reasonable yield. Because of this and because the basic block performs two logic functions simultaneously, the interconnection problem between blocks has been reduced by a factor of two to three.

Finally, the circuit is quite insensitive to parasitics introduced through the substrate because of the low impedance of the logic node. That this is so is demonstrated in Figure 25 which shows a comparison of the transient responses of the integrated and discrete version. Also, it should be noted from this photo that the propagation time of the gate is about 5 to 6 nsec.

Figure 26 shows how a MECL half-adder may be constructed. The simplicity of the circuit should be noted which is partly due to the fact that "OR" operations are performed on the common emitters and "AND" operations in the collectors. Figure 27 shows the transient responses for both a discrete and integrated half-adder. The response times are about the same as that of the gate.

To demonstrate the system capabilities of the MECL logic circuits and also to try out a number of different interconnection schemes, a parallel-parallel adder and an adder-multiplier using

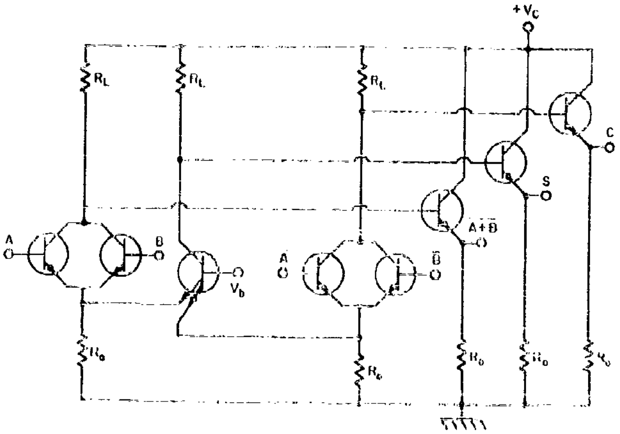

+V_C
R_L
R_L
R_L
C
S
A+B̄
A
B
V_b
A
B̄
R_o
R_o
R_o
R_o
R_o

Figure 26 - Basic Circuit for Integrated Half-Adder

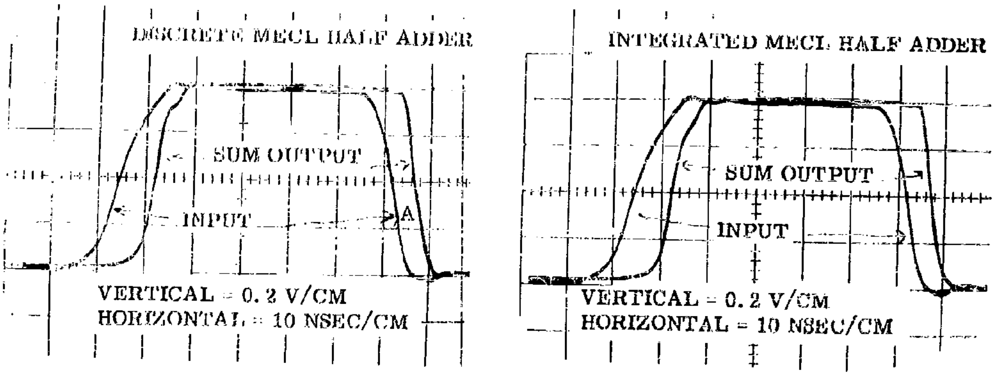


Figure 27 - Performance Comparison of Discrete and Integrated Half-Adder

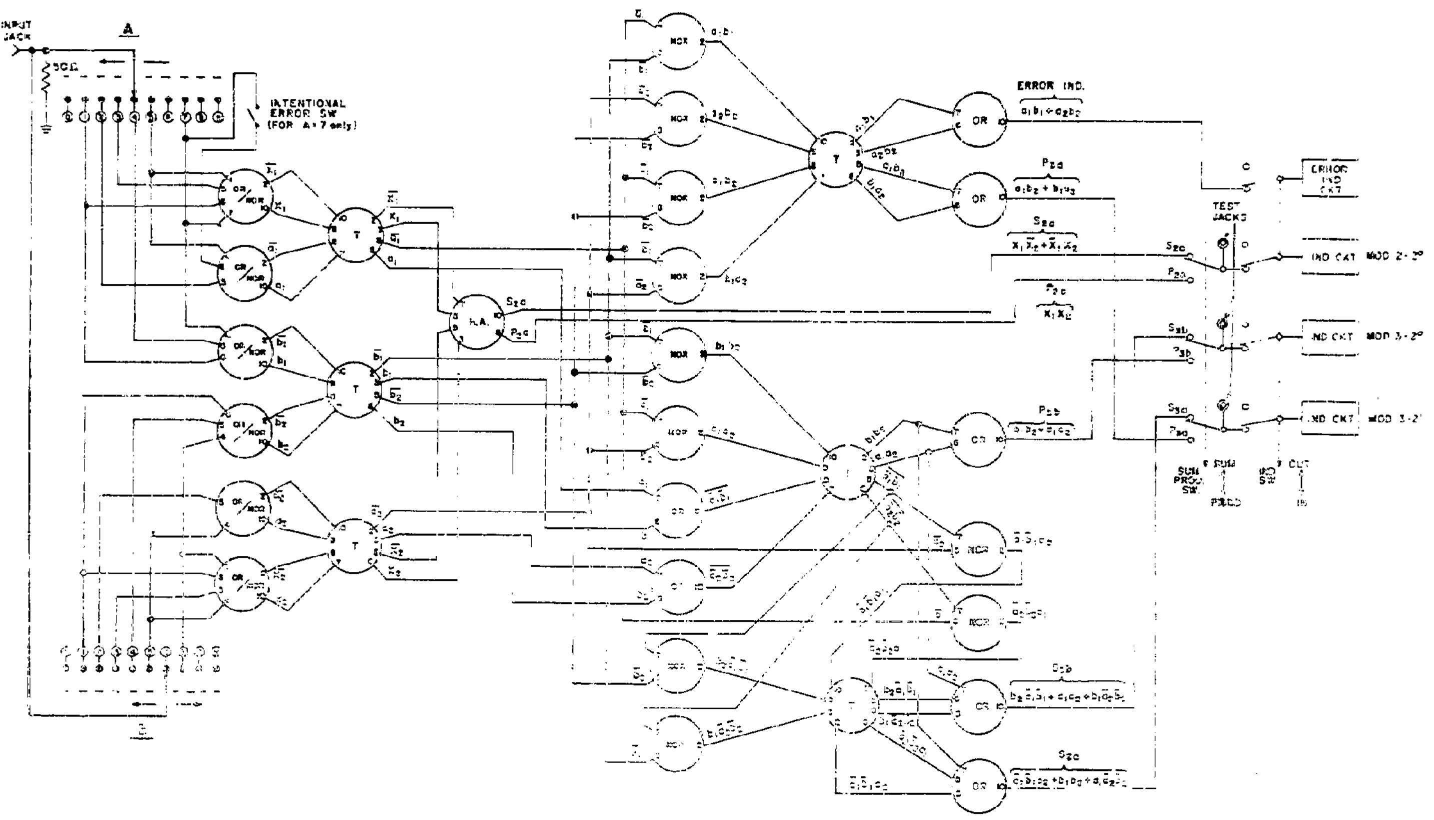

INPUT JACK
A
50Ω
INTENTIONAL ERROR SW (FOR A=7 only)
OR/NOR
T
H.A.
NOR
OR
ERROR IND.
$a_1b_1+a_2b_2$
P_{2a}
$a_1b_2+b_1a_2$
S_{2a}
$x_1\bar{x}_2+\bar{x}_1x_2$
P_{2c}
x_1x_2
P_{3b}
S_{3b}
S_{3a}
P_{3a}
TEST JACKS
ERROR IND CKT
IND CKT
MOD 2-2°
MOD 3-2°
MOD 3-2'
SUM
SUM PROD SW
PROD
IND SW
OUT
IN
B

Figure 28 - Functional Block Diagram of Error-Detecting, Residue Number System Adder-Multiplier

the residue number systems was constructed. The block diagram for the adder-multiplier is shown in Figure 28. The two numbers to be added or multiplied are fed into the switches, A and B, at the very left. These numbers are then translated into the residue number system and then added or multiplied. The adder-multiplier also has an error detecting scheme built into it which turns on an indicator light if any errors occur. For the residue number system, the bases 2 and 3 are used so that the adder-multiplier is capable of performing operations on any numbers between zero and six. Figure 29 shows the transient responses at the sum and product output for the most significant digit of the base 3, which incidentally, is the digit which requires the largest number of logic operations. It can be seen that the total delay is about 30 nsec and since 5 logic decisions are involved between input and output, this means that the average time spent on each logic decision is about 5 nsec.

Figure 30 shows a fully integrated version of the MECL "OR/NOR" gate. This is the one for which complete process was shown.

Figure 31 shows the entire adder-multiplier on one 2" x 2½" ceramic.

I have discussed in detail a rather advanced logic circuit design now in production in integrated form at Motorola. It is the fastest logic circuitry available today in either discrete or integrated form.

I have done it, not really to take advantage of this opportunity to advertise our product, but in order to expound the philosophy that guides us -- the philosophy I believe in completely -- even when we and others have designed logic blocks to supersede these we are now making.

The philosophy is this: We have available to us today a new technique. To optimize that technique one does not just copy the circuits of yesterday and build them in integrated form. It is necessary to do more than this. We must be creative -- we must invent new circuits and new approaches to achieve our basic building blocks which minimize the limitations of our new techniques and maximize the advantages of this new technology.

Then, and only then, will we be in a position to really use this new technology in order to take a giant step forward.

This, incidentally, brings me into a position to make a remark about efforts that are already extant to standardize integrated circuits today.

I personally feel that this would be a mistake. We are still groping around and I feel at least a year -- and perhaps two years -- should elapse before we begin to standardize.

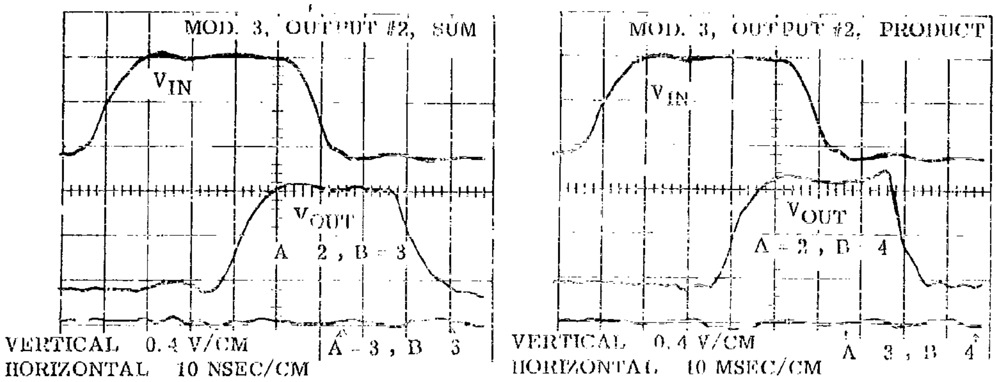


Figure 29 - Comparison Between Input and Output of Residue Adder-Multiplier After Signals Have Travelled Through Five Logical Levels

Figure 30 - Universal Logic Circuit

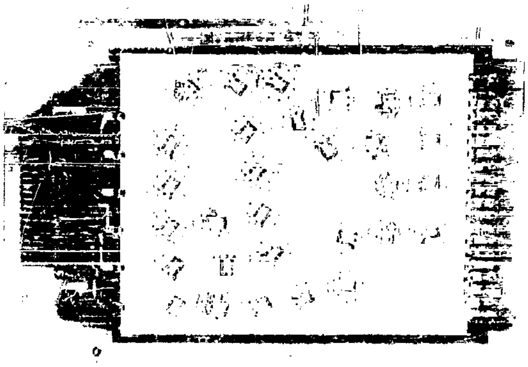


Figure 31 - 30-Stage Adder-Multiplier Reduced to 2 x 2-1/2 Inch Dimensions Through Integrated Circuit Technique

If a few circuits are picked for standardization today, the commercial incentive will require us to put larger amounts of engineering effort on building these cheaply and in quantities. As a result, I am afraid our total progress in the right direction -- wherever that might be -- will suffer.

Today, most, if not all, integrated building blocks are essentially analog versions of already commonly used logic circuits built out of separate components. Therefore, the design of an integrated logic block is executed by first designing the separate component version and then successfully modifying the design until one has a reasonably accurate model of the integrated version.

However, in order to take full advantage of the potential of integrated circuits, it would be desirable if one could design directly from logic to device, thus eliminating the intermediate circuit step. This is, at the present, quite far from being realized because of the inherent difficulties in the solution of the non-linear static and dynamic equations. To obtain a transient response, for instance, systematic design procedures had to be derived from the solution of simultaneously non-linear differential difference equations. As a start, one such approach is now being investigated at Motorola.

To increase the yield, redundancy probably will have to be built into the logic circuits in the future. This will be particularly true when realization of more complex logic blocks are realized which, as far as I can see, is the only way we can go in order to obtain a reasonable solution of the interconnection problem. Theoretically, this means that logic circuit will more and more often be designed statistically rather than on a "worst case" basis. Finally, I also firmly believe that adaptive type circuits or adaptive type networks will find more and more frequent use in the future. It is interesting to note that this means that the present day testing area at the end of production lines will, in the future, be expanded by adding to it a teaching station.

However, it should be pointed out that arguments against redundancy and adaptability have been ventured. For instance, it can be argued that methods for switching standby circuits into action may be less reliable than the circuits themselves. Nevertheless, neurological networks in animals and humans has used both redundancy and adaptability for millions of years with apparent success.

The Impact of Integrated Circuits Upon Computer Organization

The design of a computer involves the technology of many disciplines. This is best illustrated by the so-called computer ladder;

Application
System Organization
Computer Organization
Logic Design
Circuit Design
Component Development
Physical Laws and Principles

A quick inspection of the above ladder will reveal that the Application will influence the System Organization which, in turn, will influence the Computer Organization, the Logic Design, the Circuit Design, the Component Development, etc. It can also be seen that a similar chain reaction can progress in the opposite direction. The Physical Laws and Principles will influence the Component Development which, in turn, will influence the Circuit Design, which, in turn, will influence the Logic Design, the Computer Organization all the way to System Organization.

As a result there is an interdependence of all these subdisciplines upon each other. For example, though we had a computer organization, in the works of Mr. Babbage, we didn't have a corresponding technology to implement it. This computer organization waited for a long time till the relay circuits, vacuum tube circuits, and transistor circuits technologies became available for its realization. In the future modern day technological progress will tend to "integrate" into one subdiscipline the three distinct subdisciplines of component development, circuit design and logic design.

If the early computer technology of gears and relays is disregarded, then the recent, present, and future computer technology can be separated into three distinct eras.

1) Vacuum tube circuit technology

2) Transistor circuit technology

3) Integrated circuit and logic technology

In order to arrive at quantitative, as well as qualitative conclusions, a comparative analysis is necessary. The ideal case would be to examine existing computers with similar organization and capacity that has been implemented by all three types of technologies. However, no reasonably large integrated circuits computer exists at the present so all we can do is to compare a vacuum tube machine with one built out of transistors and see if we can detect a trend that is applicable to an integrated circuit machine. For a comparison I have selected the IBM 650 and the IBM 1401 machines since these are very similar in organization and specifications. In the following table are listed the improvements ratios resulting from such a study:

Computer Volume	5.2 times
Air Conditioning Unit Volume	19.0 times
Computer Weight	5.6 times
Air Conditioning Unit Weight	30.0 times
Computer Area	3.0+ times
Air Conditioning Unit Area	6.3 times
Computer Power Consumption	18.5 times
Air Conditioning Power Consumption	42.0 times
Air Conditioning Capacity	62.8 times
Memory Access Time	8.3 times
Add Operation Time	5.3 times
Multiply Operation Time	5.1 times
Divide Operation Time	5.5 times
Purchase Price	1.75 times
Monthly Rental	1.19 times

If one imagines the 1401 machine built out of MECL integrated circuits and assumes that the propagation delay over interconnections are on the average the same as that of the circuits, and if one assumes that the memory can be improved as much as the arithmetic unit, we obtain the following improvement ratios:

Computer Volume	100-120 times based on 1401
Air Conditioning Unit Volume	Air Conditioning not needed
Computer Weight	40-50 times
Air Conditioning Unit Weight	A. C. not needed
Computer Area	5-10 times
Air Conditioning Area	A. C. not needed
Computer Power Consumption	15-20 times

Air Conditioning Power Consumption	A. C. not needed
Air Conditioning Capacity	A. C. not needed
Memory Access Time	15-20 times
Add Operation Time	15-20 times
Multiply Operation Time	15-20 times
Divide Operation Time	15-20 times
Purchase Price	2.5 times
Monthly rental	3 times

The improvements of the purchase price and the monthly rental have been derived by assuming that each integrated circuit did on the average the same amount of work as that of four transistor circuits and that each integrated circuit costs about $10.00. From the above tables the following conclusions may be drawn;

The volume of the computer will be tremendously affected. Computers like Stretch which occupy a number of rooms could probably be packaged in one or two desk sized cabinets. This volume reduction will be of tremendous value in space and air borne applications. The volume reduction is due to smaller circuits, tighter packaging, and to the elimination of the air conditioning units. Also, as a result of the increased volumetric efficiency, fewer frames will be needed to house the computer and a large amount of structural hardware will be eliminated. For instance, interchassis harnessing will be reduced considerably, thus eliminating the use of many costly cable connectors with their associated problems. Finally, reduced size will make it possible to replace much of the cumbersome back panel wiring with printed circuits interconnections, thus facilitate more efficient production and trouble shooting techniques.

The weight of the computer will be decreased 40 to 50 times which is, of course, also very desirable in missile application. The reduction in weight is mainly due to the elimination of air conditioning, smaller power supply, and reduced size of circuits and hardware.

The reduction of power required, which in itself is very desirable, has many other implications. First, it reduces the size of the power supply which represents from 30 to 50% of the total weight of a computer. Heat dissipation is lowered, so less or no cooling gear is needed, resulting in saving of space and weight. The operating temperature of the computer will be less, resulting in less failures and increased life time. Finally, the computer may be more effectively encased, thus reducing failure mechanisms due to dust, dirt, humidity, etc.

Further inspection of the above tables reveals that the use of integrated circuits will reduce the process time of various operations such as memory access time, add time, etc. by 15-20 times. Since the input - output equipment and the human operators using the machine will then represent serious limitations as to how efficiently a machine may be utilized, time sharing type programs which enable the machine to process several problems simultaneously will be used more and more frequently. This, in turn, will give more impetus to the development of more efficient data reduction units and display devices which will enable the operator to digest the output data more rapidly and communicate more efficiently with the machine. Teleprocessing on a large scale will be the eventual outgrowth of this development in which a large number of customers are connected by wire or microwave relay link to a centrally located supercomputer. Since such a computer would have to be extremely complex, very reliable and very fast, it is not too far fetched to conclude that integrated circuits technology will play an important role in the realization of such a machine.

The use of integrated circuits will also have a revolutionary influence upon the computer designer's thinking because they will enable him to incorporate into the computer organization methods, techniques and number systems which were prohibitive yesterday due to the large amount of hardware needed for their implementation. For example, the operation of addition, which is done parallel by bits and serial by digits in most computers today, will become a parallel by bits and digits operation; thus reducing add time by several orders of magnitudes. Another area in which the parallel operation could be used to advantage is in the matrix compare operation for pattern recognition.

The area of error detecting and error correcting, the duplication of data paths and the "look ahead" type of operations which are avoided in most present computer organizations will find more frequent use in the future. Their inclusion will tremendously improve present day reliability standards.

Use of number systems other than binary, such as weighted or fixed bit code systems (which are avoided because of their implementation) might also become more popular.

So far all innovations mentioned have been in the hardware portion of the computer. Integrated circuits might influence the software portion even more. All the computer organization tried so far were chosen for their hardware simplicity and consequently lower cost. Suppose some integrated circuits configuration would make it possible to implement at the same cost a computer that could be organized around some numeric or alphanumeric system which would be simple from the programmer's point of view and the programing language used instead of hardware simplicity. This would enable people to talk to computers much more easily and the computers to understand the outside world much better. Analytical computers which manipulate algebra and calculus the same way humans do might even become practical.

A very important factor in computer design is the time it takes to develop a computer which presently varies from one year to seven years. The introduction of integrated circuits might considerably reduce that time. Suppose the computer designer is in a position to order "off the shelf" a number of standard logic function blocks such as adders, registers, buffers, rings, clocks, counters, and control sequencing units which corresponds to microprograming and macroprograming units. Then the computer designer will be able to arrive at a computer organization in the same time it takes to develop, say, an adder today. In view of the fact that today only a short time elapses before a piece of equipment is obsolete, this would indeed be a very desirable step forward.

To sum up, the computers of the future will be smaller, lighter, less power consuming, faster, and more parallel in their mode operation. Although they will be much more complex, they will be more reliable and it will be much easier to communicate with them. I am convinced that integrated circuit technology will play no small part in the realization and development of such machines.

The Interconnection Problem

During my discussion so far I have carefully and purposely avoided any lengthy discussion of the interconnect problem. What is worthwhile to say about this most baffling problem, except to state that considerable amount of homework remains to be done. However, I would like to take this opportunity to answer a question that is so often asked of semiconductor people when they are giving a paper on some topic in connection with integrated circuits. The question usually goes something like this:

> "Instead of trying to diffuse a more complex circuit into a piece of silicon or trying to develop a faster integrated circuit, why don't you guys concentrate on the interconnect problem?"

I think the answer to this question is obvious. Through the development of more complex and versatile integrated circuits, and by improving packages for the circuits, the semiconductor industry is contributing their share toward a solution of the interconnect problem. However, to solve this complex problem completely we need the help and cooperation of system and equipment manufacturers. Only through the joint efforts of systems and device designers can this most baffling problem be solved.

In closing, I would like to point out that the work reported here is the product of dozens of people at Motorola. I cannot list them all, but would like to single out Jan Narud, Arnie Lesk and Glen Madland for special acknowledgment. These three individuals have been instrumental in advancing our technology to the present high level.

ONR AND NAVY BUREAU REPORTS

Chairman: N. J. Smith
Office of the Chief
of Naval Operations

Department of the Interior
September 26, 1962

NAVY LABORATORY MICROELECTRONICS PROGRAM CONFERENCE

Introductory Remarks
by
Bureau Session Chairman
N. J. Smith
Office of the Chief of Naval Operations
26 September 1962

Gentlemen:

Since World War II, the Navy has been seeking methods and techniques that will improve the reliability of electronic equipment. Tinkertoy and the Army Navy Instrumentation Program are representative of this type of work. The Navy has also investigated the feasibility for commonly used functional circuit standardization, as a step towards maintenance simplification and spare parts reduction. This work is typified by the "Preferred Circuits" supported by Bureau of Aeronautics at the Bureau of Standards and the work on electronic functional division standards that was supported under contract by Bureau of Ships. These programs are considered very necessary and have always been fully supported within available resources by the Office of the Chief of Naval Operations. Although these programs contributed towards the objectives for improved reliability and circuit standardization, the proper incentives for incorporating these concepts into Navy equipment were lacking.

Over two years ago, extensive surveys of the work on microelectronics that was supported in industry, was made by ONR and BuShips. The results of these surveys made it readily apparent that the interest for microelectronics in industry was very strong. These studies also indicated that reliability was an inherent attribute in the technique and furthermore the fabrication processes and the economics were favorable towards circuit standardization. It was these factors that encouraged the Navy to support a microelectronic program at its present level and furthermore to implement microelectronics into forward going research and application program.

Yesterday was devoted to the research and development programs that are supported by the Navy under contract. Today we will continue with the research and development programs but we will also include the steps that the Navy plans to take towards implementation of microelectronics.

MICROELECTRONICS RESEARCH
SPONSORED BY ONR

E. H. Hurlburt
Office of Naval Research
Washington, D. C.

Electronics has in a sense been with us nearly a hundred years starting with the first applications of electrical devices for power, light and transportation. It began to flower into its present highly complex form in about 1920 with the advent of radio broadcasting. The ideas of microelectronics go back only fourteen years to the first appearance of the transistor. This is only about two years younger than the Office of Naval Research.

This and related devices have developed rapidly and it has seemed to me convenient to describe the present and future activity in the form of the spectrum of progress shown (Fig.). We start on the left with packaging as in micro-modules, then thru integrated circuits of both the thin-film ceramic substrates and semi-conductor substrates and we reach the functional blocks on the extreme right. The powers of ten represent in orders of magnitude the density in number of conventional components per cubic foot possible in each area. On the right conceptually the figure could exceed the $10^8/ft^3$ indicated. These regions which are limited by the first solid and dotted line delineate those portions of the spectrum which involve concepts ready or in the dotted portion nearly ready for practical use. The second line indicates the regions where basic research is needed but less extensively in the dotted portion than in the right hand solid portions. This third line indicates the regions in which the principal efforts of each of three military services has been concentrated, although indeed a portion of the efforts of each Service have been in the other areas as well.

It is not necessary before this audience to review the general character of the techniques involved. It perhaps should be recalled that the making of inductive components is still quite a challenge in the art, and that active elements in thin film form are a research objective, perhaps closer than we think, judging from Mr. Selvin's paper yesterday.

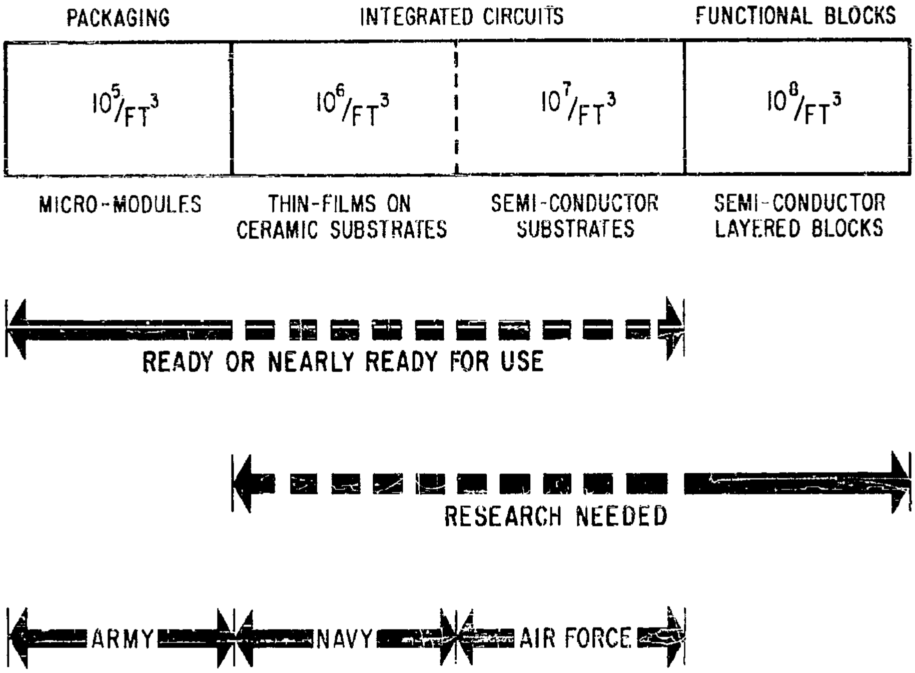

PACKAGING
INTEGRATED CIRCUITS
FUNCTIONAL BLOCKS
10⁵/FT³
10⁶/FT³
10⁷/FT³
10⁸/FT³
MICRO-MODULES
THIN-FILMS ON CERAMIC SUBSTRATES
SEMI-CONDUCTOR SUBSTRATES
SEMI-CONDUCTOR LAYERED BLOCKS
READY OR NEARLY READY FOR USE
RESEARCH NEEDED
ARMY
NAVY
AIR FORCE

Figure 1

I must emphasize again that smallness per se is neither the only nor the most important goal. Reliability achieved through the large number of intrinsic internal connections in the integrated form and the possibilities of redundancy is the most important objective of Navy microelectronics.

Lest one be carried away too far in our enthusiasm, we must remember that some areas of electronics will probably remain highly intractable to microelectronics, such as: for example, high power devices, inputs to systems as antennas where gain and frequency considerations usually dictate apertures, and outputs designed for humans require gauges, displays, tapes, etc. of a size matching man's limited capacities.

I now wish to describe briefly the contract program in microelectronics of the Electronics Branch of the Office of Naval Research.

At the California Institute of Technology research is being conducted by Professor Mead on the use of so-called "hot" electrons to produce active devices. In these, for example, a Tantalum film has a covering layer of insulation, Tantalum oxide Ta_2O_5, and over this a conducting film of gold. In the presence of high field gradients energetic or "hot" electrons cross or tunnel through the insulating barrier. This results in a type of diode in film form. Research on the temperature dependence of the voltage-current characteristics is being conducted.

Also at California Institute of Technology under Professor Gould the characteristics of thin super conducting films are being investigated with emphasis on surface impedances. This is a relatively new direction in this program.

At the University of Southern California research directed by Professor Kapriclian is under way to measure the microwave resistances of thin films in an apparatus in which after being vacuum deposited on portion of a disk the film can be rotated directly into a wave guide for measurement without being exposed to the outside atmosphere. The films will eventually be cooled in a cryostat so that their properties in the superconducting state can be measured in situ.

In another contract at Stanford University, Professor John Linvill whom you heard yesterday developes theoretical models of microcircuits and fabricates practical realizations of them.

At the Brooklyn Polytechnic Institute, Professors Carlin and Silber deposit ferrite films 600°A thick which exhibit non-reciprocal properties of potential use at microwave frequencies.

Two universities presently under contract have developed excellent film technology laboratories. These are the University of California at Berkeley under Professor Pederson and Carnegie Institute of Technology under Professor Williams. Here research can be conducted in a university atmosphere but having opportunity for interchange with related investigations in the industrial complex close at hand.

And finally, the contract program at RCA-Princeton should be mentioned. This work was described in detail yesterday by Mr. Stanley and further comment would be redundant. There is in the Applications Group of ONR a program actively looking at the impact of micro-electronics in the 1970 era ship, addressed to the "gray" box concept.

Having briefly discussed the present contract research program, I wish to look a-ways into the future and describe possible directions of research. Probably the most obvious and frequently emphasized is general material research. This has as one goal the discovery of new knowledge of the solid state of matter which can be formulated and applied in microelectronics. Another goal is to seek new combinations and applications of old knowledge of solid state physics to yield functional block micro-electronic devices.

This area is not being neglected in our program for basic research, in fact solid state studies are included in the contract programs supported by the three services at Harvard University, Massachusetts Institute of Technology, Stanford University, and of course the work under Professor Bardeen at the University of Illinois is an ONR contract.

The results of these university researches, as well as those I listed earlier appear in widely disseminated technical and progress reports and eventually also in the published literature familiar to all of you.

In planning research certain special avenues should not be neglected. An example is the use of controlled and programmed electron or ion beams to deposit exceedingly minute components in atomic or molecular layers from a plasma source. In concept conducting, semi-conducting and insulating materials could be deposited from appropriate plasmas yielding passive and active components of unprecedented fineness in detail. It is known that a number of groups are working on this approach. This and similar unique avenues of research should be pursued.

Now to turn for a moment to a topic which I once thought might seem remote to this Conference but it has been already raised by earlier speakers so without hesitation I shall talk a little about bio-electronics.

This is a two way street for research. Microelectronics provides instrumentation of minute size and delicate form by which the behavior, physiology and nervous systems of animals and humans can be investigated. Small, light weight electronics packages can be attached or imbedded in animals or humans to tele-meter behavorial or metabolic information. Delicate probes can be implanted to record nerve and brain impulses, or conversely the probes may be used to actively stimulate the nervous systems of the animal or human subjects. A portion of the Electronics Branch contract at the Research Laboratory of Electronics at the Massachusetts Institute of Technology is applied on their extensive program of neurophysiology. An example of the output of this work was the detailed study of the responses of the retina of the frog's eye. A surprising congruence of the electronically derived information with the micromorphology of the retina was revealed. Thus clearly the output of micro-electronics furthers bio-electronics and the rapidly advancing research in physiology, neurology and medicine.

But as I said before, this is a two way street, since from advancing biological research there is feed back to micro-electronics in the form of new concepts in computers, self-organizing systems and data processing arising out of our newly gained knowledge of neurophysiology. The current study of the long twisting helical strands of the deoxyribonucleic acid molecule which contains the basic genetic information for all living things has revealed that it may be described as a binary coded number that may run to 100,000 digits in a single strand. This vast amount of information is reliably encoded and stored. I repeat, reliably, we're here aren't we? And with this brief contemplation of the DNA molecule, I will conclude my remarks with the observation that here already is information storage on a vast but minute level beyond the present dreams of the microelectronics engineer but inspiring him with the knowledge of what can be done.

MICROELECTRONICS RESEARCH PROGRAM FOR INFORMATION PROCESSING
in the
OFFICE OF NAVAL RESEARCH

Richard H. Wilcox
Head, Information Systems Branch

The Information Systems Branch of the Office of Naval Research is concerned primarily with new or improved methods, devices, and techniques for processing information. We have no program in microelectronics as such, pursued as an end in itself. There is no line item in our budget entitled, "Microelectronics". Nevertheless, in our pursuit of improved information processing, we find that a substantial portion of the investigations we support do in fact qualify quite properly as members of the ultra-Lilliputian fraternity. This is not because we particularly want small components--in fact, we would usually prefer to avoid them as a matter of convenience--but rather because the constraints of fabrication costs, large-system reliability, and propagation time demand size reduction and monolithic structure.

In particular, we have found it pertinent to support investigations of thin films, both magnetic and cryogenic, and of electron-beam activated micro-processes. We have also several devices or processes under investigation which are at present "normal" sized but may turn out to lend themselves to miniaturization for applications in which that appears to be desirable. This latter class includes, for example, magneto-strictive memory devices, ferroelectrics, electron spin-echo memories, and neuristors.

But reduction-in-size and function-integration cannot be considered in isolation from other areas of technology; not, at least, if we wish to utilize such techniques in real-world information processing systems. At least two other areas of research must be pushed in parallel for the early realization of practical microelectronic hardware. The first of these stems from the economic necessity of fabricating simultaneously large numbers of micro-elements. Probability theory and experience tell us that we must expect something less than perfection in fabrication processes, and common sense tells us that exhaustive individual testing of myriad microscopic devices, followed by repair or replacement of bad units, is completely impractical. Thus systems incorporating such elements must either utilize a form of redundant logic or else exhibit a capacity for self-diagnosis and healing. Neither approach has received anything like adequate attention. The second requisit "peripheral" research area stems from somewhat similar considerations: our conventional philosophies of hardware design and operational maintenance are woefully inadequate for the treatment of systems comprised of many millions of inaccessible, microscopic elements. Such systems defy the imagination to conjure up realistic estimates of operational capabilities and constraints; this is one reason why more and more investigators are looking to biological systems to suggest feasible avenues of progress.

While we are considering such tremendously complex systems of micronic elements, it is germane to note that electronics per se does not form the sole means of implementation. Optics lends itself nicely to certain modes of miniaturization, as is illustrated by fiber optic techniques. Fluid digital devices are not yet in the class with some of the smaller integrated electronic circuitry, but they are getting smaller and they promise real competition from the standpoints of economy and reliability. One can conceive of chemical processes being tamed for purposes of processing information. Perhaps our ultimate systems will turn out to be electro-chemical--as in the human nervous system.

The Information Systems Branch cannot hope to cover all of these important areas of research with anything approaching comprehensiveness. At the moment we have about a quarter of a million dollars invested in support of research which is properly classed as microelectronics, with perhaps a third that amount going, in addition, into directly supporting areas such as redundancy techniques and large systems organization. We might argue, of course, that all of our work in adaptive and self-organizing systems is relevant, since large self-organizing systems demand mass fabrication techniques for economic reality and, conversely, self-organization is a prime candidate for solution of the problems of large-system design (by "learning", or self-design) and maintenance (by continuous adaptation). However, we will limit ourselves here to those research tasks which fall within the conventional bounds of microelectronics and its direct support. Note, however, that--in keeping with our Branch objectives--these tasks are oriented toward information processing rather than to a better understanding of microelectronic principles per se, although the latter is usually a highly desirable by-product of the work.

In the area of thin films, we have at the Systems Technology Laboratories two complementary tasks. One is concerned with thin-film cryotrons and their combination into useful circuitry, including considerations of mass fabrication and ultra-miniaturization; the other concerns the realization of associative computer memories by means of cryotron circuitry. A related effort at the RCA laboratories is investigating cryogenic thin-film implementation of content-addressed computer memories. And in the magnetic thin film area, we are supporting at the Laboratory for Electronics a study of domain wall phenomena.

The Stanford Research Institute is conducting a substantial investigation of the potentialities of electron-beam-activated processes. In contrast to the ion-beam idea for depositing miniaturized circuits, the SRI approach utilizes a sharply focussed, rapidly deflectable electron beam to supply energy for local chemical activation of materials previously deposited on a substrate, thus permitting the rapid "writing" of extremely minute circuitry. Densities in the order of 10^{10} elements per cubic inch may be ultimately obtainable with this technique, with the specific circuit "layout" being governed by a computer program which controls deflection of the electron beam.

In the microelectronics support areas, the Systems Research Group is conducting for us a carefully controlled theoretical and experimental evaluation of the capabilities and limitations of majority logic, and the Westinghouse Electronics Division is engaged in the development and comparitive evaluation of a variety of other redundancy techniques. Finally, the National Biomedical Research Foundation is looking into the potentialities and problems which would be encountered in computers having in the order of 10^9 logical gates.

As this short enumeration of our program tasks demonstrates, we are doing only partial justice to the important areas of research in microelectronics. In addition, funding constraints require constant reevaluation of even this insufficient effort as it competes for dollars with our other areas of responsibility in the information sciences. As this audience is certainly well aware, research in microelectronics tends to be relatively expensive because satisfactory fabrication is difficult to achieve, required instrumentation is complex and often unique, and extensive experimentation is required.

Let me conclude by offering a few observations concerning what we consider to be neglected areas of microelectronics. There exists today a wide variety of miniaturized devices, components, and even sub-systems, but they have for the most part been developed empirically. Thus their capabilities and limitations are not well understood, and little if any design data exist to guide modifications or development of new devices. Similarly, we have an impressive array of sophisticated theories concerning various solid-state phenomena, both bulk and thin-film, but the limits of validity of these theories and the soundness of the assumptions upon which they rest are, in many cases, highly questionable. I have no wish to discourage the mad scramble to invent more devices and utilize additional physical phenomena, but let us also invest some money and time in the definitive evaluation, explanation, and delineation of the devices and phenomena we have already, so that we can select those most appropriate to our needs and improve them efficiently.

MICROELECTRONICS PROGRAM AND PLANS IN THE BUREAU OF SHIPS

G. W. Neumann
Bureau of Ships
Code 361B1

Gentlemen,
there are two subjects I wish to discuss this morning. First, is a brief summary of the work the Bureau of Ships is supporting in developing microelectronic techniques and devices; and some of the areas in which we are applying these devices. The second deals with proposed plans for a program in which microelectronics can play a major part. We are unveiling this program to industry for the first time today not in an attempt to give industry firm guidelines as to how we will design electronics equipment in the future, but rather to give you an idea of the way in which our studies indicate we should go and to obtain any suggestions you may have.

First let me summarize our current efforts in microelectronics. The Naval Electronics Laboratory, San Diego, is our lead Lab in this field. The work at NEL is applications oriented - especially in computers systems. They have used RCA micromodules to construct a "P" time counter" in an NTDS detector - tracker console. These devices have been operating in this console for several months without failure.

They have applied Fairchild micrologic elements and Texas Instruments solid circuits, as well as, PSI and General Instrument integrated circuits to a medium-sized programmed computer, with varying degrees of success. They have contracted with RCA to build a test set fabricated entirely from micromodules. They are building a binary to decimal converter and reader. Part of this circuitry is being built using six different conventional and microelectronic circuit approaches thus allowing direct comparison of various techniques.

The Material Laboratory located at the New York Naval Shipyard is working on developing and evaluating general useage analog assemblies. They are presently attempting to have 11 of these assemblies produced using microelectronics techniques.

In addition, they are working on simplifying fault location techniques for equipment using these assemblies.

At the Naval Research Laboratory we are supporting basic investigations of the physical & electrical properties of new semiconductors devices as well as developing new and improved devices and circuits. In particular they are assisting the Bureau in evaluating commercial work in thin film active devices.

In the commercial field we are supporting a number of tasks. Westinghouse has developed prototype models of high voltage switching devices using planer diffused techniques for an electrolumenescent display system permitting a significant decrease in size, cost and cabling over present designs which use silicon controlled rectifiers.

Another significant task Westinghouse is undertaking is the development of a family of microelectronic general usage assemblies for use in the construction of five equipments which compose a large portion of the shipboard central time and frequency control system. This system is particularly adaptable to this type "Standardization" since many of the circuits are similar, and many of the equipments are still in developmental stages. The purpose of this project is to optimize within this system the number of assemblies needed, and to compare the relative merits of various microelectronics fabrication techniques. As you heard yesterday both Lear and Sylvania are working on techniques for developing entire thin film assemblies, the main problem being obtaining reproducible active devices using vacuum deposition on dielectric substrates. Sylvania is also developing a tape control unit for use with a medium sized-medium speed computer. This tape unit, with the exception of the power supply, is being completely developed from micro-circuits and will be approximately 20X20X9 inches. Three-quarters of this volume is taken-up by the power supply. On another contract, Sylvania is working on a military application of crystal growth of silicon by epitaxial methods. This is to develop controllable and reproducible growth techniques from the vapor phase in order to provide multiple junction structures.

We have a contract with Motorola to develop thin-film techniques for use in depositing inductive elements on ferrite substrates and then depositing ferrite films over the conductor. An inductive range of 38 microhenries to 1 millihenry at 1 MC is desired.

CBS Labs in Stamford are conducting research and development of tunnel diode devices and arrays capable of operation at microwatt power levels by use of electron-beam technology and automatic video programming.

This has been a brief summary of some of the work this Bureau is sponsoring.

Now, as I stated before, the second subject I wish to talk about is a proposed program which is still in the planning stages. We call this program PRISE, which is the Program for Integrated Shipboard Electronics.

This program we feel is the answer to a number of problems facing the Navy today. The advance in weaponry - faster planes - faster missiles- more striking power - has developed a requirement so great that the human element must be supported by sophisticated, and many times, complicated electronics. Because the human element of command-control must make rapid, complex decisions and they must be the best decisions, the electronics support must be the best - it must work when needed.

The moment when our nearby friend yells "Head-Up" is the moment for which we design our electronics - it must not fail - it must be there working at full capability.

Electronics today has been swept up in an ascending spiral of equipment complexity, longer lead times, increasingly poor electronic maintenance, poor equipment reliability, and an involved logistics problem.

The spiral is the inevitable result of equipment sophistication. Under conventional electronic design and production practices, equipment conceived in this room today may not be in the fleet by 1970.

Today there are many approaches to solving this problem. These include using various microelectronic techniques, automatic test equipment, ultra-reliable parts, modular design, throw-away assemblies, and so on. The solution to one problem usually causes new problems in another area.

As an example, why aren't our system design engineers taking full advantage of the benefits offered by microelectronics today? One of the answers is that these circuits provide a logistic problem. Each individual circuit must have one or two spares stocked aboard ship. Most of these circuits would be designed for one specific equipment. Without volume production the cost of spares becomes prohibitive. This points out that present approaches are piecemeal. They do not solve the problem of producing warfare systems which will meet military operational requirements at a cost the nation can afford.

We feel something is needed -- A comprehensive approach to the design, production, installation, operation and maintenance of electronic systems. The approach must consider the costs of new methods initially and throughout the life of the equipment. It must consider logistics of war and peace. It must be acceptable to both Government and industry.

We think the answer is PRISE, the Program for Integrated Shipboard

Electronics. Hardly one element of this program is entirely new or radical. It has all been tried before -- in pieces -- with varying degrees of success. But never together, integrated, coordinated.

PRISE is composed of three elements:

- The PRISE Pack Program, aimed at development of truely general-usage functional packages, PRISE packs.

- The System Availability Program, aimed at the optimum application of advanced reliability and maintenance techniques, applied to system design to assure availability of systems when needed.

- The Integrated Ship Program, involving application of the first two elements to the design of an entire integrated ships electronic suit.

PRISE PACKS

First, I would like to discuss the PRISE pack program. The PRISE pack is a general usage functional assembly. Its complexity will probably compare to todays one or two stage conventional circuit. It will perform basic electronic functions, such as audio amplification, oscillation and the like.

As shown in figure 1 the basic concept of PRISE packs, as contrasted with conventional technology, is this: while conventional electronics is based on the piece-part as the basic element, PRISE will employ the PRISE pack as the basic functional element. Packs will be interchangeable, electrically and physically, with other packs performing the same function. Groups of PRISE packs will be suitably interconnected to form the next increment of assembly, the maintenance module.

What makes this proposed program different from others of this type? Flexibility! The PRISE pack program is flexible. It permits and encourages advances in technology and is adaptable to current and future developments in packaging and microminiaturization. We assure this flexibility in three ways.

First, packs will be described in terms of performance only. We are interested in electrical inputs and outputs; transfer functions; physical size and shape; type of connections; and environmental and reliability characteristics. Once a pack is developed and we are assured our requirements can be met, what's inside the package is of little interest, especially to the systems designer. We do not plan to dictate manufacturing techniques. This we feel is industry's job. Packs could contain tubes, transistors and parts, or microelectronics circuitry. This provides the microelectronics industry the chance to compete in performance and cost with other more conventional fabrication techniques.

Secondly, we envision truly general-usage packs--packs that can be used in a variety of electronic equipments, systems and environments. Certain arbitrary decisions must be made by the Navy to arrive at pack performance characteristics. Mistakes will be made, but the program must be dynamic--flexible enough to correct errors; able to incorporate state-of-the-art advances, with a minimum of disruption; and able to use general usage packages developed outside this program.

And last, we recognize that not all circuitry is amenable to pack design. Studies have indicated that 60 to 80 per cent of shipboard electronic circuitry could use PRISE packs. The remainder is unique circuitry and there appears to be no advantage to using the pack concept.

The advantages of PRISE packs appear rather obvious.

- Reduced Lead Time and Reduced Development Costs:

The use of PRISE packs will eliminate much of the time required for design, testing, and production of electronic systems. We will no longer spend money to redesign the audio amplifier. We will not need both breadboard and service test models in the design stage. We will not have to re-engineer for production. Equipment assembly will be simplified. Once a reasonably complete line of packs is available 50 per cent reduction in lead time seems very probable.

- Improved System Reliability: Volume production of PRISE packs will afford the opportunity of establishing more effective controls to yield uniform quality and predictable performance. Rapid accumulation of test and operational experience will provide firmer reliability guarantees to the builders of systems using a high proportion of packs. Volume usage of PRISE packs in equipment and system design will justify using larger samples for reliability assurance testing. When larger samples are tested, test costs and time requirements become more economical.

- Improved System Maintainability: The use of PRISE packs will reduce the number and variety of circuit functions to be learned by the maintenance technician. Trouble shooting will be simplified by permitting fault location at the functional circuit level. Parts - level fault location will be eliminated for purposes of first-line maintenance. Automatic test equipment will become far more flexible and useful as a maintenance aid, since test points, conditions, and criteria will be standardized.

- Simplified Logistics: A limited number of PRISE packs will replace a wide variety of conventional assemblies, components, and parts. This will reduce the number and cost of spare parts in the supply system.

The second important part of the PRISE program is called system availability. System availability is defined as the probability that an electronic equipment will be available for use when needed. We propose to achieve a high level of systems availability by the use of automatic test equipment, by optimizing the trade-off between maintainability and reliability, and by logistic considerations which may include the use of throw-away packs, rear echelon repair of maintenance modules, and things of this nature.

The real serious problem that we have in Navy today is the fact that only 7% of the ET's we train in "Navy A" school re-enlist. Most previous efforts of electronic maintenance training have been in the direction of modifying the man to fit the complicated job we have set for him. The system availability part of PRISE is a program to modify the Job to fit the Man. PRISE demands that test equipment, educational material, maintenance aids, techniques and trained technicians be ready at the same time the equipment is ready.

Previous military experience with automatic test equipment has been somewhat disappointing. We have attempted too much with one piece of equipment and quite often this results in an improper allocation of functions between man and machine. As shown in figure 2 the concept of automatic test equipment to be employed in the PRISE program is this: Centralized system elements, appropriately distributed, that will be able to check the entire electronics suit; maintenance action will be taken down to the maintenance module level. Separate equipment off-line will test maintenance modules and individual packs quite like tube testers presently do.

I have spoken of the trade-off between reliability and maintainability. By careful consideration of the reliability of available PRISE packs and by the use of active redundancy, it can be forseen that certain types of equipment could be 99% maintenance free for periods up to four months -- essentially maintenance free at sea.

As I stated previously, PRISE is still in a planning stage. However, a number of our tasks, such as the development of the central time & frequency control system, are using many of the PRISE concepts. So, it is not a question of using these concepts, but rather to what degree will they be used. I feel that to prove the true worth of this program it must be applied to an entire shipboard electronic suit. This vehicle could be one of our future integrated ship designs, or it could be an experimental ship much like Admiral Roeder described yesterday.

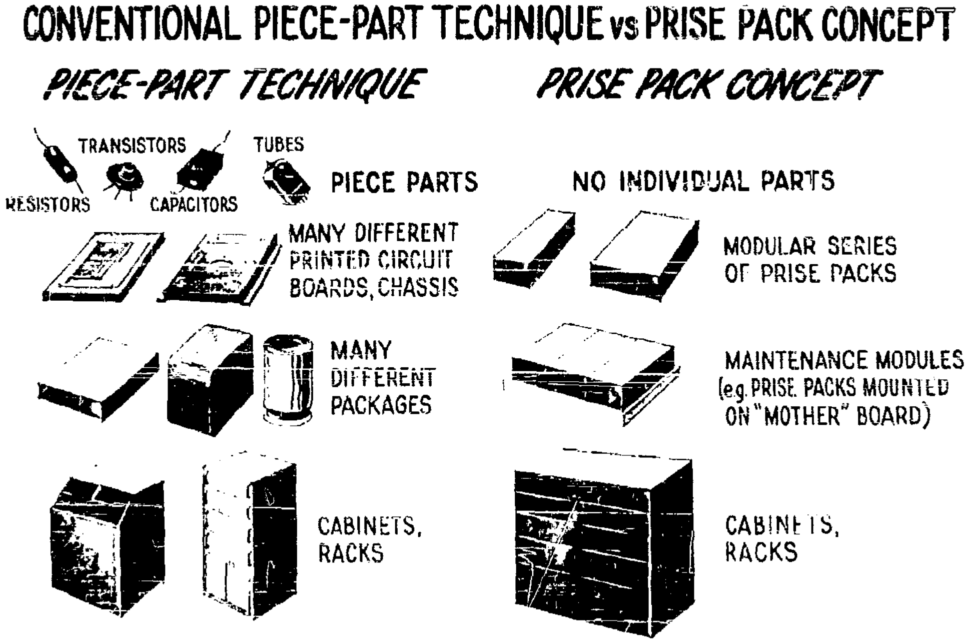

CONVENTIONAL PIECE-PART TECHNIQUE vs PRISE PACK CONCEPT
PIECE-PART TECHNIQUE
PRISE PACK CONCEPT
RESISTORS
TRANSISTORS
CAPACITORS
TUBES
PIECE PARTS
NO INDIVIDUAL PARTS
MANY DIFFERENT PRINTED CIRCUIT BOARDS, CHASSIS
MODULAR SERIES OF PRISE PACKS
MANY DIFFERENT PACKAGES
MAINTENANCE MODULES (e.g. PRISE PACKS MOUNTED ON "MOTHER" BOARD)
CABINETS, RACKS
CABINETS, RACKS

Figure 1

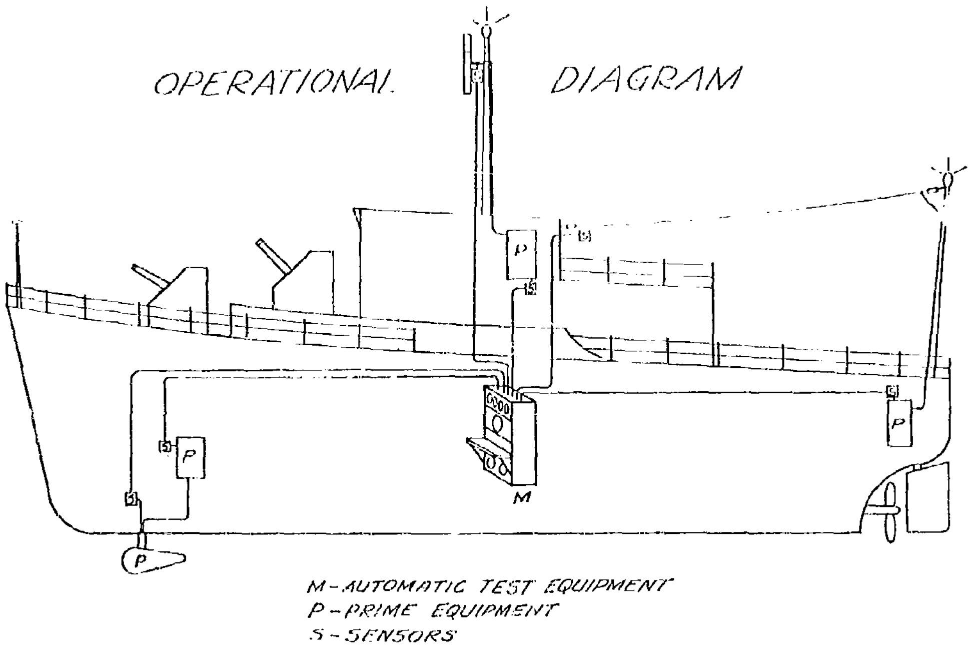

OPERATIONAL DIAGRAM
P
S
M
M - AUTOMATIC TEST EQUIPMENT
P - PRIME EQUIPMENT
S - SENSORS

Figure 2

A THIN FILM ELECTRONIC SUBSYSTEM FOR MISSILE APPLICATIONS

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The merits of thin film microelectronics for missile systems, or other such militray systems, has been expounded by many organizations (including the Applied Physics Lab). Up to the present time, however, only small pieces of hardware have been built for evaluation in military systems. The next logical step is to choose a relatively large electronic system and have it fabricated to military specs. using thin film techniques. The goal of the effort I am going to discuss here is to take this next logical step. We, of the Applied Physics Lab, have recently initiated a program to fabricate, using thin film circuitry, an entire electronic subsystem of one of our missiles. If the subsystem passes all preflight tests we plan to fly it with the eventual intent of incorporating the subsystem into our flight hardware.

Before proceeding further I feel I should state our reasons for choosing to build this subsystem using thin film circuitry rather than with bulk semiconductor circuitry.

1) We believe the present state of the art of thin film circuit fabrication is more advanced and more flexible when fabricating custom made electronic systems.
2) The speeds and pulse risetimes of thin film circuitry is much higher than in bulk semiconductor circuits.
3) The lead time to fabricate the system from the circuit design is much shorter.
4) We did not want to pay for any circuit redesign which would be absolutely essential if bulk semiconductor techniques were to be used.
5) We wanted to evaluate the possibility of employing large amounts of thin film circuitry in our systems.

The first step in this type of program is to choose an electronic subsystem that is compatible with present state-of-the-art thin film fabrication techniques. This means it should probably be a digital system since the types of components and their values are most compatible to thin film circuit fabrication. Also, digital systems usually consist of many redundant circuits which is important. Again the choice of the electronic system is very important; otherwise the advantages of thin film circuitry can be entirely lost.

A simplified block diagram of the subsystem we chose is shown in figure 1. The subsystem is actually a large decoder which provides two types of output functions. An example of a switching output might be to turn a power supply on in the missile while an analog output might be to deflect a missile fin a given amount. Only one output will exist for a given set of input digital information.

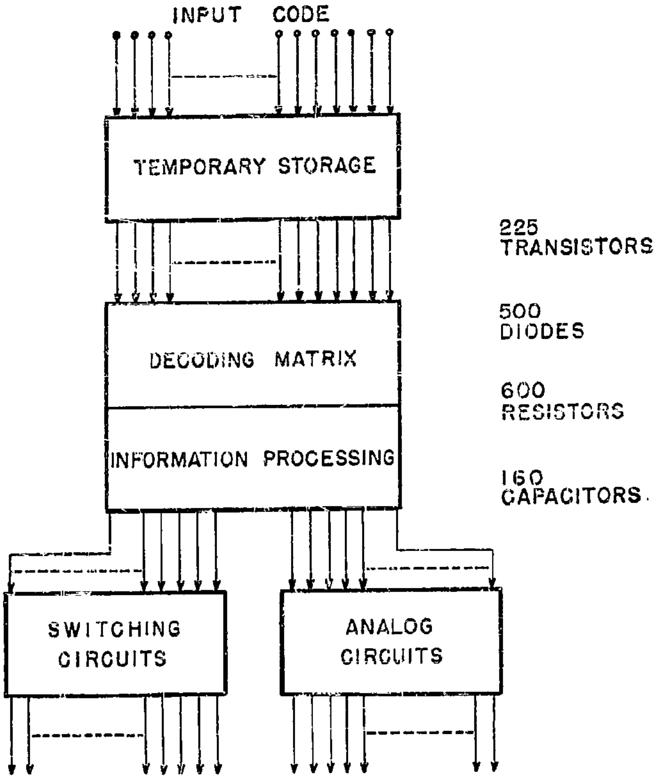
This decoder system has been designed down to the last detail by the Applied Physics Lab and has been thoroughly breadboard tested. The entire schematic diagram will be given to the thin film fabricator therefore reducing to a minimum the amount of engineering design that he must perform. The subsystem, as indicated in figure 1, contains 225 transistors, 500 diodes, 600 resistors and 160 capacitors for a total of approximately 1500 components.

The next step was to write the specification for the fabrication of the system. This is probably the most difficult step since it is the most ambiguous. The specification must be written so that the finished subsystem will pass all performance specifications, yet not restrict or inhibit the type of thin film fabrication procedure that the fabricator wishes to employ. We believe it is too early in the game to specify the material and procedure that must be used or even the shape or size of the circuit substrates or modules. We did, however, lay down certain ground rules. A few of the more important ones I will mention here:

1) All passive components must be filmed and the tolerance of the components must be filmed to within ± 5% without trimming.

   There was one exception to this spec. and that is that any capacitor larger than .01 ufd could be attached to the circuit.

2) The circuits must be filmed using a continuous, compatible series of operations which can lend themselves to eventual production operations. We do not believe for example, that half-way through an evaporation procedure the circuit should be removed from the vacuum system chemically treated in solution and then reinserted into the vacuum


INPUT CODE
TEMPORARY STORAGE
DECODING MATRIX
INFORMATION PROCESSING
SWITCHING CIRCUITS
ANALOG CIRCUITS
225 TRANSISTORS
500 DIODES
600 RESISTORS
160 CAPACITORS.

THIN FILM DECODER

Figure 1

FAST FLIP FLOP
(FFF)

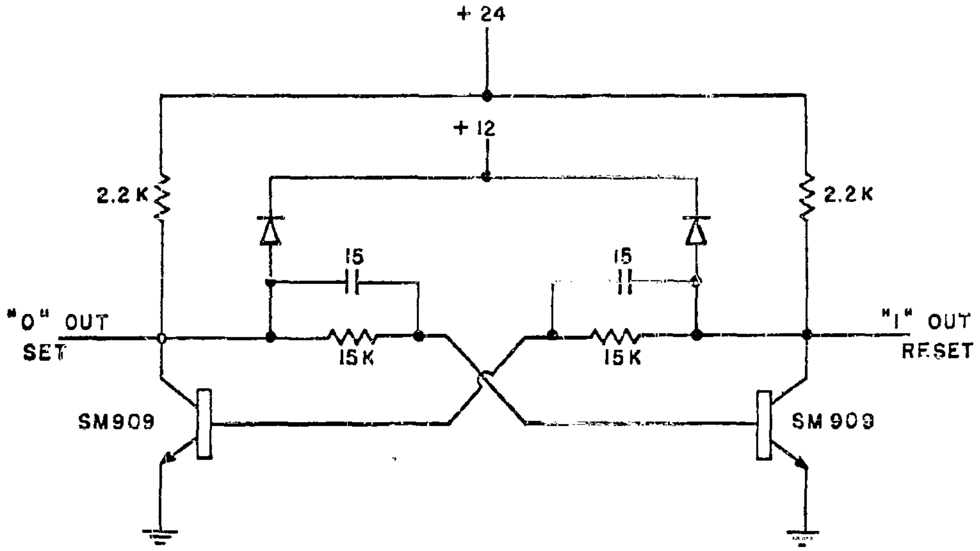

+ 24
+ 12
2.2 K
2.2 K
15
15
"0" OUT
SET
15 K
15 K
"1" OUT
RESET
SM909
SM 909

Figure 2

system to continue the fabrication.

3) All transistors and diodes may be attached to the substrate after all the components have been filmed, however, they should be an integral part of the packaged module.

4) The cost of the transistors and diodes of a "minimum servicing package" or throwaway package should not exceed $150.00.

5) The subsystem must operate satisfactorily when subjected to the specified environmental condition.

6) A delivery time of 6 months for three complete subsystems packaged to fit well within the size specifications provided.

A typical circuit of this system is shown in figure 2. All the components must be fabricated to a tolerance of ± 5% and there are no unreasonably large values of resistors or capacitors. The transistor and diode types listed are those used in the Applied Physics Lab design and the equivalent subminiature replacements will be made.

One of the perhaps more difficult circuits to fabricate is shown in figure 3. Because this is a digital-to-analog converter the resistors of the digital-to-analog resistance ladder must be fabricated to a tolerance of ± 1/2% and the two resistors of the flip-flop which drives the ladder to ± 1%. Since it is presently impossible to directly film resistors with these tolerances they may be trimmed after fabrication.

The Applied Physics Lab has decided to have this subsystem fabricated on contract rather than attempt to build it themselves for the following reasons:

1) The facility at the Applied Physics Lab has been established to investigate the state-of-the-art of microelectronics and to perform research on materials and techniques. It is therefore not equipped to fabricate the number of circuits required or to assemble and package a system of this size.

2) We wished to evaluate the ability of outside contractors to fabricate an entire thin film system to military specifications and adapt their technique to production methods.

The Applied Physics Laboratory sent out an exceptional high number of requests for bids -- namely 25. Approximately half the companies have responded with good responsible bids and we

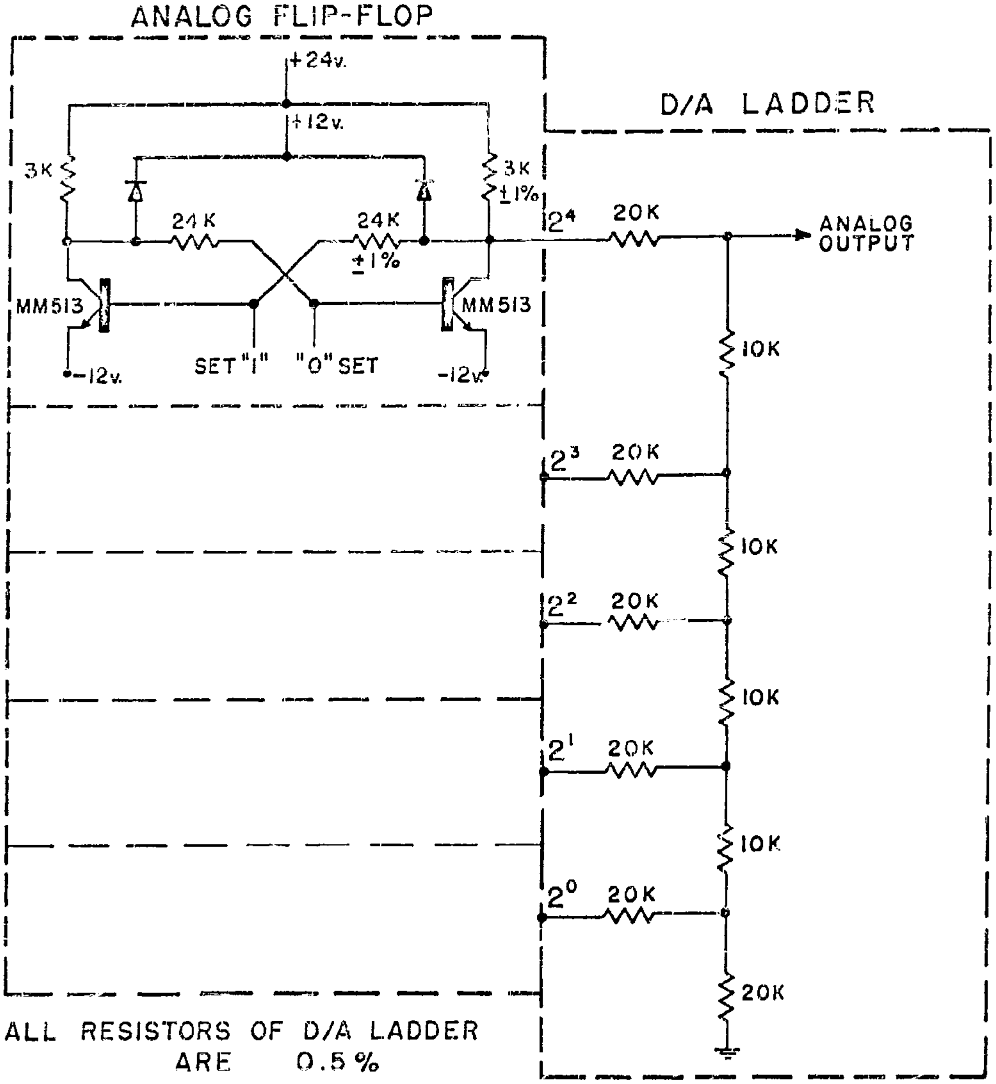

ANALOG FLIP-FLOP
D/A LADDER
+24v.
+12v.
3K
3K ±1%
24K
24K ±1%
MM513
MM513
-12v.
-12v.
SET "1"
"0" SET
2^4
2^3
2^2
2^1
2^0
20K
20K
20K
20K
20K
10K
10K
10K
10K
20K
ANALOG OUTPUT
ALL RESISTORS OF D/A LADDER ARE 0.5%

Figure 3

shortly expect to grant the contract to one of these. The subsystem we have chosen is one that we need in one of our missiles system. It is presently being built using welded technique; therefore this thin film fabrication effort is being conducted in parallel with the welded effort and if successful will replace the welded unit.

In conclusion, there are a number of things we have thus far learned:

1) Many companies are willing and able to fabricate the subsystem that we desire.

2) The environmental conditions under which the system must operate present absolutely no problems and the indications are that the system should be even more reliable than the equivalent welded unit.

3) The cost of fabricating a single subsystem (after the initial tooling and the problem of fabricating the first few units have been worked out) is compatible or less than the cost of the equivalent welded subsystem.

4) The size and weight of the packaged thin film system is about 1/3 to 1/4 the size of the welded system. This size reduction could be much greater if one of our important goals were to make it as small as possible.

5) The cost of a throwaway module can easily be kept to a reasonable value (perhaps $250) without undue hardship or sacrificing quality.

EFFECTS OF NUCLEAR RADIATION ON ELECTRONIC EQUIPMENT

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ABSTRACT

The data used in this paper are derived from two previous papers given at the SAE Convention in 1961 and at the WESCON Conference in 1960, and updated for presentation at the Microelectronics Conference.

Nuclear radiation interacts with matter - - - The strength of the interaction varies with the nature of the radiation. Neutrinos, for example, interact so weakly that experimenters doubt that the interaction can be detected. Charge particles, on the other hand, interact strongly and dissipate their energy in a very short path. Gamma rays and neutrons, with which we are primarily concerned, interact with intermediate strength, producing charged and neutral particle recoils. The strength of interaction can be related to the mean free path for scattering out of a beam. Typically this distance in air at STP is about 400-500 yards for gamma rays and 250-300 yards for fast neutrons. Charged particles interacting strongly with matter dissipate their energy rapidly and consequently have more or less well defined ranges which are short compared to the mean free path for neutrons and gamma rays. Radiation effects in materials result from the energy deposited by means of interactions leading to ionization and to recoil and nuclear disintegration particles. The energy deposited is commonly called the "dose". It is measured in terms of a variety of units, each appropriate to some peculiar field of investigations, e.g., roentgen, rep, rem, rad, etc. The utility of these terms is not always clear to the experimenter. Lewis Carroll anticipates this situation in "Through the Looking Glass":

> "When I use a word," Humpty Dumpty said, in a rather scornful tone," it means what I choose it to mean - neither more nor less." "The question is," said Alice, "whether you can make words mean so many different things." "The question is," said Humpty Dumpty, "which is to be master - that's all."

All these units measure the radiation in terms of the energy deposited in a specific material without regard for the details in the process of energy deposition. Because the detailed process involved in the interaction of radiation with matter is frequently of essential importance to the understanding of effects, dosimetric techniques must be augmented by physical measurements of radiation flux. In fact, if the radiation flux measurements can be made in sufficient detail, the dosimetry becomes a part of the theoretical computation process. Practical difficulties, however, dictate that both types of measurements be made. Dosimetric measurements and calculations are necessary to take into account the perturbations in the radiation field that are produced by the presence of the experimental material. Radiation flux (and spectrum) measurements are necessary to provide the basis for computation of detailed effects. These requirements should become clear later in this discussion.

Permanent radiation effects are related to the total radiation dose. Such "dose" effects are changes in the mechanical, electrical, and optical properties of materials. Very extensive studies of dose effects have been made for the sake of reactor materials. Typically one observes changes after irradiation in physical properties at dose levels greater than a megarep (rep = radiation that deposits 100 ergs per gram of material). A megarep is approximately equal to 10^6 roentgens.

Since the median lethal dose (MLD) for humans is in the order of 500 r, it seems that one should not be concerned with the radiation vulnerability of manned equipment, since materials effects begin to appear at a dose 2,000 times that required for the median lethality in humans.

"Dose effects," in the ideal case, are independent of the rate with which the dose is delivered. Transient conditions in an experimental sample are considered to be in equilibrium with the radiation and to disappear completely by the time the effect is measured after the radiation and thus are not observed in before-and-after measurements. If the irradiation time is long (the rate is small), the idealized conditions for observation of "dose" effects are approximately met.

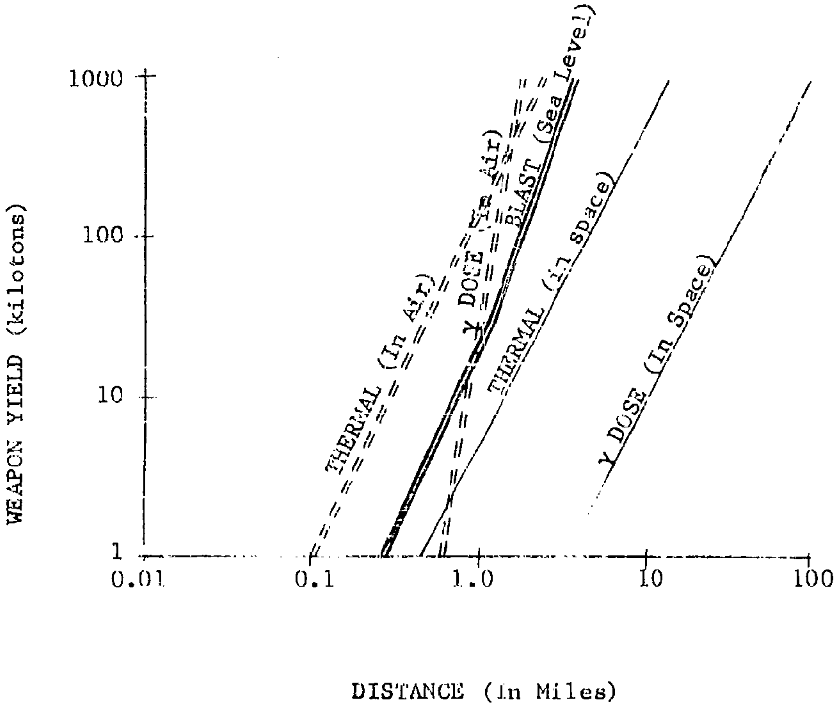
Directing our attention to the other extreme (i.e., consideration of transient effects only), we can distinguish two cases: the rate effect is an observable in equilibrium with the radiation rate - it disappears when the radiation ceases; the relaxation effect is an observable not in equilibrium with the radiation rate - it depends on the time constants of the phenomenon observed, i.e., the rate with which the rate effect comes to equilibrium with the radiation rate.

In principle, we may relate all three cases to relaxation time; the dose effect corresponds in the limit to finite relaxation time; the rate effect to zero relaxation time; and all other transient effects to finite relaxation times.

The radiation environment of a reactor is a steady state. Rate effects can be studied in a reactor by observing physical properties during the irradiation. However, the peak radiation rates are not great enough to provide a reasonable simulation of the weapon environment. There are, however, quasi steady state environments of concern: the Van Allen bands; cosmic rays; slowly varying radiation belts from solar flares; and the environs of an unshielded reactor. The study of transient radiation effects, however, is brought to importance as a result of the transient radiation fields in the neighborhood of a nuclear weapon detonation. "The Effects of Nuclear Weapons" (S. Glasstone, Ed., Publ. USGPO $2.00, 1957) describes the sources of the initial nuclear radiation from a weapon. Neutrons released in the fission process that are not absorbed in the chain reaction leak out. Gamma rays are attributed to three processes: fission, including inelastic neutron interactions with the bomb material; neutron captures in nitrogen; and decay of radioactive fission fragments. The gamma rays emitted during the fission process represent a small percentage of the total gamma ray flux - about 1 per cent according to the reference quoted above. Since the fission proceeds for only a very short time, the gamma rays are emitted at a very high rate. The August 8, 1960 issue of AVIATION WEEK presents the range-versus-yield at which gamma ray peak rates of 10^7 r/sec can be expected. Since these ranges are rather large (Slide 1), one may expect peak rates for future equipment ranging from 10^7 to 10^{10} r/sec for exposure at ranges within the published contours.

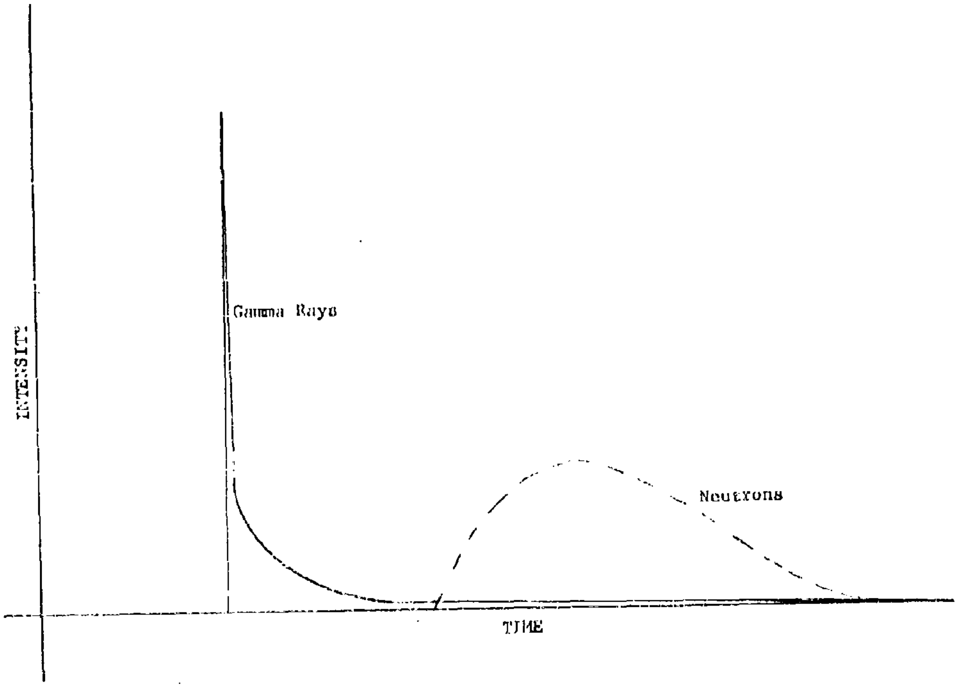
The gamma ray peak rate falls off as the inverse square of the distance. The neutron peak rate, however, falls off as the inverse cube of the distance because the neutrons are born with a distribution in velocity. Thus, at large ranges, the neutron peak rates and total fluxes will be small while the peak gamma ray rate remains relatively large. A typical time history of radiation near a weapon is shown in Slide 2.

The foregoing statements serve to justify the emphasis I will now place on the study of transient radiation effects resulting from high peak rate pulses of gamma rays. They serve as an introduction to outline the jargon and provide a basis for the discussion of experiments directed toward understanding transient radiation effects.



AIR BLAST: 5 lb/in^2
INTEGRATED THERMAL FLUX: 100 calories/cm^2
PEAK γ DOSE: 10^7 roentgens/sec

Slide 1



Slide 2

Our interest in this field would be merely academic were it not for the fact that system vulnerability presents a threat to reliable system performance in transient radiation fields. The possibility that malfunctions can occur which do not result from permanent (or dose) radiation damage stimulates study of the basic effects. Whole system studies have been made, and potential failures have been observed. Although it has not been possible to subject systems to radiation pulses intense enough to simulate small ranges from weapon detonations, the response of systems to available laboratory radiation pulses indicates that sophisticated systems are vulnerable. The study of failure potential in the actual environment is required to evaluate the operational penalty paid for transient radiation vulnerability.

The fundamental interactions between radiation and matter lead to effects which can be divided for convenience into two categories: the re-orientation or displacement of electronic charge which relaxes very rapidly and is thus specifically a transient effect, and the displacement of atoms within the lattice - the production of defects - which is a relatively long-term or permanent effect. Permanent effects which can be observed in terms of circuit performance degradation do not begin to appear until the accumulation of a very large dose. One possible exception to this is that transistor performance is affected by integrated fluxes of neutrons in the order of 10^{12} neutrons/cm^2. The range from a nuclear detonation at which such doses of neutrons are delivered is very small compared to the range at which intense pulses of gamma rays are delivered. Thus, at relatively large ranges in which there is no dose damage to operators or to humans, and at which there is relatively small dose damage to transistors from the neutrons, the gamma ray peak rates can be 10^6 r/sec or higher, and vulnerability to transient radiation effects becomes the primary concern.

The transient effects which involve the displacement of electronic charge can again be divided into several categories, one of which is the production of leakage paths in the gas surrounding the component, in the potting material, or in the substrate upon which the components are built. Another phenomenon of radiation effects is that due to the injection of charge by gamma rays through the photoelectric and Compton processes. This effect appears as the equivalent of a current generator injecting currents at some point in the component. Finally, in active components, the displacement of charge within the component can take place in such a way as to disturb its performance. For example, in the transistor, the charge produced in the base region endures for a time which is dependent upon the minority carrier lifetime. Such disturbances show the time constants of the component, the circuit or the material, rather than the time history of the radiation pulse itself. The magnitude of the effects is in some cases dose-dependent. Dose dependence can be observed only when the radiation pulse is exceedingly short compared to the lifetime of the electronic phenomenon in the electronic component. The magnitude of the effect as a circuit signal depends upon the impedance level since a given amount of charge in a low impedance will generate a lower voltage signal than the same charge in a high impedance circuit. Some of the features of microelectronics processes appear very attractive for the production of radiation-hardened systems and components. It should be possible to minimize the leakage-effect by appropriate geometrical and mechanical design so that leakage paths are minimized and thus the interfering effect due to electronic leakage will be minimized. It should also be possible to make use of low impedance circuits in such a way as to minimize the signals that are introduced by the photocurrent effects and finally, if the substrates and component materials are suitably chosen, it should be possible to minimize injection and photoconductor effects. Here the choice of materials would be made so that electronic equilibrium is established. (This is a technique used in preparing dosimeters for reading dose under conditions in which the interaction of the dosimeter with the environment is important.) By such a choice, the charge injected into the component from the surroundings, and out of the component by the radiation will tend to be made equal.

To recapitulate: Transient effects produced by gamma rays appear at much greater ranges than any other weapon threat. These transient gamma-ray effects result primarily from displacements of electrons by ionizing processes, and by photoelectric and Compton effects. These effects produce voltages and currents in a circuit which in some cases can degrade or destroy the function of the circuit. To combat these effects, one tries to design low impedance circuits, to provide potting which comes near to electronic equilibrium, and to choose components in which photocurrent effects and charge injection are not important.

It is interesting to note as an aside that some time ago the magnitude of the effects observed in transistors under irradiation led some designers to conclude that all weapon system electronics for use in the nuclear radiation environment would have to be designed around vacuum tubes. It turns out, however, that the high impedance circuits usually associated with vacuum tubes lead to a transient effect which is larger than that observed in transistor circuits which are usually designed for low impedance operation. It is important to note at this stage that the choice between transistors and vacuum tubes is not a straightforward and easy one to make.

It will be necessary in the design of future systems for the radiation environment that interdisciplinary consideration between electronic designers and nuclear physicists be given to the process of circuit design. Some progress has been made in this area by the use of analog computer techniques applied to the analysis of circuits in which the radiation effect is considered as an integral part in the circuit analysis. The matter of primary interest in the analog computer technique is that it directs the attention to those components and those processes which make the major contribution to the transient radiation effect. For the design of specific systems, it is now customary to consider the design as produced without consideration of the radiation environment, and to designate those circuits, components, modules, or functions which are peculiarly vulnerable to radiation effects. Only those components which show vulnerability are considered for re-design purposes. Re-design can be suggested by the nuclear physicist, but will have to be made primarily by the electronic designer since he is the only one who can evaluate the trade-offs between radiation hardness and circuit performance. In the design of circuits and systems one should consider hardening for gamma ray pulses to at least 10^8 r/sec.

READYING INDUSTRY FOR THE MANUFACTURE OF MICROELECTRONICS

H. B. Parker
Asst. Head, Industrial Readiness Branch
Industrial Division
Bureau of Naval Weapons
Washington 25, D.C.

Gentlemen:

Our job in Industrial Readiness within the Bureau of Naval Weapons is to assure the readiness of industry to manufacture the future naval weapons under the varying conditions of peace, limited war or general war.

Today peace includes the technological race with our potential enemies. In this technological race we commonly hear such statements as "The Russians currently have bigger rocket motors, but we surpass them in miniature electronics technology." We have justifiable pride in our laboratory successes in microelectronics--many of which have been discussed this week. I suspect, however, that the Russians will become more concerned when these laboratory feasible technologies have been reduced to practical production machines and processes and when we engage their use in producing weapons in our competitive economic system.

Developing an Industrial Base for Microelectronics. Five years ago our long range industrial planning established a need to move our industry toward a broad microelectronic capability. How does one influence industry to go through a costly revolution such as this?

Developing "In-House" Competence. We decided to use the leadership of getting our own hands dirty first. We wanted to prove first to ourselves the production feasibility of promising laboratory technologies, once proven we would make the results available to industry without duplication of costly engineering effort. After detailed study of microelectronics state of art and in close coordination with the Navy Microelectronics Panel, the Naval Avionics Facility at Indianapolis was directed to establish a pilot production capability.

(A) To develop a technical competence in-house on microelectronics.

(B) To evaluate the manufacturing feasibility of various microelectronic technologies previously proven technically feasible in the laboratory by trying them out on weapon components under production conditions.

(C) To develop standards and specifications for the production and procurement of microelectronics.

Buy technology for general industry use. The Bureau established the policy for NAFI to buy and evaluate promising technology from industrial firms for the general use of industry. Such general technology would serve as a base line from which industry could work in further advancing microelectronics.

Current status of manufacturing technology program. Five years, much hard-to-comeby experience, and many dollars later results are beginning to unfold.

On Monday, some of you heard NAFI's Mr. Scott report on his supporting research work. Most of you heard Mr. Carroll's report on the first major guinea pig equipment which will be used in evaluating the production machines described in Mr. Stutz's paper yesterday.

From the background of these papers you can see that we are currently starting the evaluation phase of manufacturing feasibility of these Mod I machines. We expect to continue improvements within the Navy and expect industry to do the same. Furthermore, we are interested in buying more advanced technology, especially we are interested in the active element area. We want technology just as soon as it is proven technically feasible and is ready to be evaluated in a manufacturing operation.

The summary of current status then is as follows: This week microelectronic circuit elements are being manufactured using these production machines at the Naval Avionics Facility in Indianapolis to evaluate the manufacturing feasibility of basic microelectronic technologies. At IBM in Kingston, New York, company owned duplicate machines are producing prototype hardware even more advanced than discussed in yesterday's paper by Mr. Carroll. Today, other industrial firms are negotiating for additional sets of identical production equipment. Within the next few weeks press releases will announce the general availability to U. S. Industry of the complete details of manufacturing processes, details of machine design and operation, and sale of the machines themselves.

With the appearance of production equipment capable of quality re-production of quantities of microelectronic elements, we find some of our doubting Thomases are being converted to seriously consider application of microelectronics in their own system problems. This gaining of system engineering acceptance is a major step toward utilizing microelectronics in weapons.

Caution. One word of caution to industry in developing microelectronics capability. We in Military Procurement will be most reluctant to specify weapon designs which are limited to the production technology of only one firm. In our annual buys of electronics we must effectively utilize the competitive forces of our economic system. There is strong resistance to the award of long range programs that have a locked-in proprietary hold on all future production.

The Navy's Requirements in Electronics

Colonel A. C. Lowell
Avionics Division, Bureau of Naval Weapons
Washington, D. C.

It is a well-known fact that had not World War II ended when it did the logistics of supply and maintenance could not have continued to keep the expanding electronic requirements of the United States Navy in a state of ready operation. The major problem facing the fleet today, one which is becoming more severe and forbidding as time progresses, is associated with the increasing complexity in Avionics equipment with which the fleet must operate. This problem extends to that which faces the carrier division commander who may have a hundred strike aircraft under his command. He demands high aircraft availability, operational capability that must be available to him around the clock--not merely at periodic intervals. This means fully operational aircraft, fully operational ships, all of which must be capable of accomplishing their mission under all-weather conditions for twenty-four hours each day.

Indications of aircraft complexity are reflected in the tremendous growth of aircraft airframe costs from $9.00 a pound (several years prior to World War II) up to $120.00 a pound at the present time. This, mind you, is the cost for the airframe alone.

The complexity of Avionics components and other systems has also grown. Along with this increased complexity is attendent basic and ownership cost. And along with complexity and cost is the increased number of maintenance manhours that are required to keep the aircraft in fully operational condition.

Another factor that is important here is the number of hours of down time for aircraft maintenance. This time is very often dictated, not only by the complexity of the equipment that may require a certain number of maintenance manhours for its repair, but also by the number of men that are actually available to work on a given system at any time.

The adverse effects of these problems are increasing with time. There is still another factor which is presenting an additional limiting capability on the Navy's overall effectiveness, and this is the reduced experienced manpower capability to which the Navy has access. This specifically limits the fleet's maintenance capability for the equipment which the Fleet must operate. This restriction is one that is not only limited in terms of numbers, but is restricted in terms of educational and training capabilities which are required in connection with the maintenance and operation of complex equipments for the entire fleet. All these factors combine to degrade mission effectiveness. Their solutions demand decisive, sharply directed effort.

To further appreciate the extent by which these factors are affecting the Navy's mission effectiveness and which, in effect, constitutes the basis for mission degradation, let us look at the increase in the time for which aircraft are unflyable for the purpose of maintenance. In looking at current fleet aircraft, those types which were introduced to the fleet some five to six years ago, require about 50% down time for maintenance. This means that, out of every twenty-four hours, approximately twelve hours are required for maintenance and the up-keep of the equipment sufficient to keep it fully operational for the remaining twelve hours. As we proceed to more modern aircraft which were introduced to the fleet some two to three years ago, the requirements for maintenance have increased. Not only has the total time increased to about 60%, but the number of manhours of maintenance per operating hour has also increased.

In our most modern aircraft, which are being introduced into the fleet at this time, as a result of the complexity of the aircraft equipments, the aircraft are actually operational or flyable for only 25% of the time. This degraded condition is not improving, and there is nothing on the horizon at the present time, employing existing techniques, that promises to ease this problem. In each of these cases, down time for avionics maintenance contributed most to the total down-for-maintenance time.

Examining why this situation exists, we look at the measure of growth in the complexity of equipment which can be reflected by examining the number of active element groups in an aircraft such as the AD airplane that was operational and considered one of our first line attack airplanes back in 1952 and 1953. At that time, this aircraft had a total number active element groups of around 250. An active element group, as a measure of Avionics complexity, can be a diode, triode, a transistor, or a vacuum tube with associated connections. Proceeding with time, we see that the A3D2, introduced into the fleet in 1958 had a total number of active element groups of slightly over 560. Proceeding to our more modern aircraft, the total number of active element groups has increased on the order several hundred percent. The growth in complexity is increasing exponentially. This is a measure, not only of complexity--

it is also a measure of increased equipment and ownership costs, of increased requirement for maintenance, and an indication of increased time required for maintenance.

In the case where an individual component may require 40 maintenance manhours per flight hour or operating hour, it is not merely a matter of putting 40 men to work on this particular component and expecting that it will be repaired in a period of one hour. There are basic limits which are imposed by the design and construction of the equipment itself which dictate the amount of time that is required for maintenance of these equipments. It can be seen that major design improvements are essential in order to introduce a significantly improved degree of reliability and mission effectiveness not only for the basic equipments but for the entire aircraft system.

In looking at another aspect of the problem, and this is something that presents one of the most severe limitations on the capability today, we must look at the capability we have for the maintenance of the equipments which we are introducing into the fleet.

Here we have a specific limitation because we are limited not only in numbers but also in the intelligence level of the young men who are available for military service who come into the Navy.

The Navy requires that, of the total naval strength which is approximately 585,000, that approximately 50% possess an IQ sufficiently adequate to enable them to complete the qualification courses necessary to maintain the complex equipment which the fleet operates.

These are reasonable requirements considering the complexity and the types of equipment which the fleet must operate in order to possess a high degree of mission effectiveness. The Navy, needless to say, as is the case with the other armed services, has not been able to fulfill these personnel requirements. In this connection, the demand for highly talented, intelligent and competent young men is increasing whereas the availability of this type of young man for extended duty beyond his four-year enlistment is diminishing. The Navy faces another major problem, in that in the technical areas, a young man who receives the training and the education which has been formalized within the Naval Service qualifies him as a maintenance man in the aviation electronics area. The Navy expends approximately two out of four years in order to give him this capability. This training will be sufficient to qualify him as a rated enlisted man. It will give him the rating, for example, in aviation electronics of an AT3. Considering that his total service time will be four years, this means that he will have only two years remaining during which he will be productive to the operating fleet. At the conclusion of this two-year period, he will then have an opportunity to re-enlist or to leave the naval service in order to obtain a civilian job in industry where he will be able to earn more money than he could earn in the naval service, or to seek higher goals through obtaining a college education. This is the course of action that our young men are taking most frequently. In coming to grips with more immediate problems and one of which the naval service along with other services must face during the next few years, the requirement for experienced avionics maintenance personnel is increasing whereas the number of personnel available who have received training and who possess experience is diminishing to a dangerous degree.

The group of men who entered the naval service during World War II during the period from 1941 to 1945 and who represent the hard core of experience in the technical fields, will be leaving the naval service upon completion of 20 years of active duty during the next three years. This constitutes a significant percentage of the maintenance capability in Naval Aviation today. By December of 1965, the Navy will have lost approximately 50% of the rated avionics electricians who are in the Navy today. Thus, whereas complexity and maintainability requirements for avionics equipments are increasing, the numerical strength of our experienced maintenance personnel is diminishing. This personnel limitation is fully as severe to the Navy as the dollar limit in connection with the procurement and operation of fleet equipment.

Recapitulating these problems which bear on mission degradation, we see that aircraft readiness must be improved by reducing the total times planes are down for avionics maintenance. The equipment reliability must be greatly improved. A 5-15% improvement is not sufficient. A major breakthrough in the meantime between failures on the order of a 1,000% is required. Maintenance manhours per flight hour must be reduced drastically. Not only must the total number of maintenance manhours per operating hour for the equipment be brought down, but also the level of training required by avionics maintenance people must be reduced. In short, a major breakthrough is needed. Requirements for test equipment, support equipment, and spare parts must be reduced sharply.

It has been shown that the total cost or ownership of the lifetime of a piece of equipment will vary from four to ten times the initial cost of the equipment. This is an area where the major savings to the Department of Defense and to our Nation can be realized. Costs must be brought down, this means the total lifetime costs of the system in relation to its operational value. Total lifetime costs includes not only the initial price of the equipment but also the special training, spare parts, support equipment, technical manuals, everything required to keep the equipment ready to go for its entire fleet life.

In analyzing the means by which improved reliability and mission effectiveness can be introduced into the avionics equipments, it must be realized that it will not be acceptable to attempt

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to reduce the capability of the avionics systems in our naval aircraft. It will not be acceptable to retrogress to systems whose capability is reduced.

The approach to greater reliability and maintainability is achieved through the application of significantly improved design techniques. This involves techniques in construction, design, and assembly--techniques directed specifically toward producing equipments of much greater reliability as well as systems which will be more maintainable within the fleet, and cost less to own and operate.

Through major advancements in electronic technology, circuit functions can now be accomplished by semiconductor devices which otherwise would require up to ten times the number of components and interconnections.

This is a revolution which has been achieved in electronics engineering. It has been accomplished not only through the efforts of scientists, but also through the efforts of physicists, chemists, ceramists, and metallurgists. Through the development of microcircuitry techniques, semiconductor microcircuits have been developed in which entire circuits including passive and active elements are contained in cans the same size as current transistor cans. These solid-state circuits are so small that they can be seen only under high magnification. The small size and weight of these circuits, however, are not the main goals. The absence of moving parts and the reduction of soldered connections reduces the major cause of electronic failures, and results in systems which are on the order of up to ten times as reliable as their conventional counterparts.

Through a disciplined employment of standard circuits among all future avionics equipment, costs per system are predicted to drop sharply.

These techniques are not in the "wish" stage. They are actually here today and are being introduced into operating equipment which is flying and which will be operational in the near future on a wide scale. These techniques have not been exploited for the purpose of reducing size and weight. Although size and weight are reduced, this is considered merely an added payoff.

The significant gain achieved through the application of these techniques is the increased reliability and attendent to this the overall reduction of costs.

The Bureau of Naval Wespons has initiated a program in which industry is being encouraged to substitute micro-circuits on a piece-meal basis in current production equipment wherever this can be done at no increase in cost to the Government. However, the first equipments into which micro-circuitry techniques have been applied is the digital navigation computer which Litton Industries

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is producing for the Grumman-built aircraft, A2F Intruder and W2F Hawkeye. Electrically equivalent plug-in micro-circuit boards have been developed to replace conventional circuit boards which hold conventional transistors, resistors, and capacitors.

Replacement of the more reliable lighter weight and, except for connector plugs, smaller size boards will actually cost less than their conventional counterparts and will ultimately result in substantial savings to the Navy in maintenance costs, not to mention significantly improved operational reliability.

These first steps are only the beginning of a four-phase program, called the MEETAT Program, designed to exploit to the fullest the improvement possibilities inherent in micro-electronic techniques. MEETAT stands for Major Improvement in Electronic Effectiveness Through Application of Advanced Techniques. Four phases of MEETAT are:

> Development of the repairable or throw-away modules, such as the replacement plug-in boards for the A2F and W2F computers.
>
> Development of the maintenance module replacement. This involves the application of modular construction of avionics equipment. Employing this construction design, these modules will be removable, less than 15 pounds in weight, and will provide for rapid fault location, facilitating the replacement of cards and the repair of accessible components.
>
> Development of functional module replacements. These are functional mission-oriented equipments. Under this phase, numerous efforts are planned and three contracts for equipment using micro-electronic and solid-state techniques have already been let. One is for an inertial guidance system to be developed by Litton Industries which is scheduled for delivery in 1964. A LORAN-C receiver to be developed by Sperry will weigh about 20 pounds and occupy a half cubic foot of space, a 75% reduction in size and weight over its present design using solid-state elements. An HF single-sideband transceiver is being developed by RCA which will be all solid-state and will weigh about 30 pounds, 70% less than its functional equivalent, the AN/ARC-38A. This phase includes the requirement for modular construction as well as visual fault location.
>
> Development of fully integrated avionic systems. Modular construction, visual fault location, standard circuits, replaceable throw-away cards

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